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High Voltage Power - GaN

## ABSTRACT

TI achieved reliable GaN products through a comprehensive in-house program ranging from epitaxial growth, application reliability validation, and the industry support of new GaN standards.

Gallium-nitride (GaN) high-electron mobility transistors (HEMTs) or field-effect transistors (FETs) are enabling an exciting and disruptive era in power conversion. The material properties of GaN have enabled power switches with much lower on-resistance and higher switching speeds than equivalently-sized silicon power transistors. These benefits are making power conversion solutions more compact and energy efficient. GaN FETs have benefited both from established reliability methodologies for silicon FETs, as well as new methodologies to validate GaN FET reliability under application conditions. This white paper describes the progress and shows that TI GaN products now have proven reliability in application.

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## 1 Introduction

For a new technology to be successful, it must be reliable in the customer application. Silicon power transistors are now regarded as reliable, but this was not always the case. Confidence in their reliability developed with longstanding experience, resulting in a well-accepted qualification methodology whereby reliability and quality are certified by running standardized tests and using reliability models for lifetime calculations. These tests were developed to accelerate failure mechanisms, with reliability engineering conducted to achieve the desired lifetime.

GaN transistors have now been known for 28 years<sup>(1)</sup>. RF GaN FETs are now widely deployed in cellular base stations. Power GaN FETs are more recent, with development efforts starting in the early twenty first century. The power GaN industry does not have the luxury of time, so has invested considerable effort to accelerate reliability development. As a result, power GaN FETs are now considered reliable and are being deployed in both commercial and automotive products.

Component level	Established framework for Si qualification and reliability	<b>JESD47, AEC-Q100, JEP122</b>
	GaN Failure mechanisms, lifetime extrapolation	<b>JEP122, JEP180</b> , literature
Power-supply level	Switching reliability for power management usage of GaN	<b>JEP180</b> : Switching Reliability Evaluation for GaN Power Devices
	GaN-specific test methods	<b>JEP173</b> : Dynamic ON-Resistance Test Method <b>JEP182</b> : Continuous Switching Test Method
	Extreme operation (Lightning surge, short circuit)	<b>IEC 61000-4-5, VDE0884-11</b>

**Figure 1-1. GaN reliability is validated by supplementing well-established standards with recent JEDEC JC-70 GaN guidelines to cover both component and power-supply level operation.**

A key criterion is the reliable product operation for a broad range of customer applications under both normal and extreme use conditions. The traditional silicon approach, does not adequately address the switching conditions of power management, so we have built upon it. Our approach is shown in [Figure 1-1](#), and consists of GaN-specific methodology to address switching reliability, conduct test, address failure modes, extrapolate lifetime, and ensure operation under extreme conditions such as lightning surge and short circuit.

The methodologies of [Figure 1-1](#) result from several other aspects important for technology maturity. First is the formation of the JEDEC JC-70 committee on Wide Bandgap Power Electronic Conversion Semiconductors, with three GaN-specific guidelines already released: JEP173, JEP180, and JEP182. Second is the creation of a body of literature on failure mechanisms and their acceleration. Third is the thought leadership around a common approach for application reliability, a challenging topic. TI has played a leadership role in all these aspects. As a result, TI GaN products incorporate a well-developed methodology to validate and assure the reliability of GaN under all conditions of operation.

The objective of this white paper is to describe the progress and methodology by which TI GaN product reliability is assured and to show results that demonstrate lifetime reliability in application.

## 2 Background

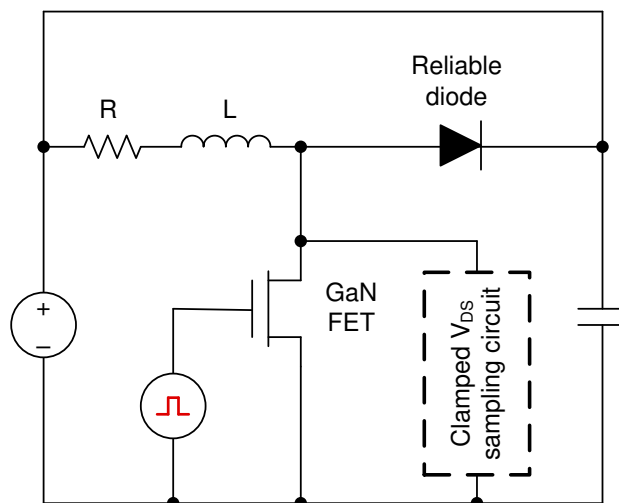
The qualification standards in use for silicon were first published in the 1990's. The popular JEDEC JESD47 standard<sup>(2)</sup>, “*Stress-Test-Driven Qualification of Integrated Circuits*” was first published in July 1995 and the Automotive Electronics Council (AEC) Q100<sup>(3)</sup> was first published in June 1994. These standards specify many tests which may be classified into three categories: device, electrostatic discharge (ESD), and package. At the time, memory and logic were the predominant applications, and the accelerated bias tests were intended to achieve an electric-field equivalent lifetime. The switching transitions of power management applications were not specifically considered.

Traditional device qualification is run by using a 1000h test at a junction temperature of 125°C or higher at the maximum operating voltage. Running at 125°C is equivalent to about nine years of use at  $T_j = 55^\circ\text{C}$  using an assumed activation energy of 0.7 eV.

Many of the tests also require a large number of parts to obtain defectivity and failure in time (FIT) statistics. For further background on traditional silicon qualification, see references 4 and 5.

Although JEDEC specifies the need for dynamic testing, conditions are not prescribed due to the ever-evolving applications and material sets in our industry<sup>(6)</sup>. The field of power conversion illustrates the difficulties. There are many different topologies and numerous components with which the GaN FET interacts. Determining the lifetime of a GaN FET in a power converter is challenging for the following reasons. First, running acceleration studies could cause many non-GaN failures. Second, the applicability to different topologies would not be clear. Third, the energy usage of running the large number of power converters needed is large. It has therefore not been straightforward to assure product-level reliability in a broad sense. As a result, traditional reliability testing has not covered the switching conditions of power management.

The need for GaN-specific reliability validation arose because traditional silicon qualification methodology was not fully addressing application reliability for GaN products. During the early days, we observed that hard-switched transitions were causing overheating and occasional hard-failure. This finding is important because a broad class of power conversion applications are hard-switched. We developed a comprehensive methodology for qualifying the reliability of GaN products, described in references 4 and 5. The papers describe a common approach of validating the application reliability of GaN FETs for a broad class of applications.



**Figure 2-1. Schematic of the test vehicle used for universal hard-switch reliability validation of TI GaN devices. Dynamic  $R_{DS(ON)}$  is measured using the clamped  $V_{DS}$  sampling circuit.**

The common approach is enabled by use of the switching locus curve to represent the type of switching stress applied to the device, and thereby the failure mechanism exercised. The switching locus curve is the trajectory of the  $i_D$ - $v_{DS}$  waveform during a switching cycle<sup>(7)</sup>. A test vehicle circuit with a hard-switching locus will therefore apply relevant stress for hard-switching applications<sup>(7)</sup>.

Our test vehicle circuit shown in [Figure 2-1](#) and described in references [4](#) and [5](#), is a boost converter stage with the output tied to the input to conserve energy. It is a similar circuit to the double pulse tester (DPT) with a different control. We use it in continuous-pulse mode for providing accelerated hard-switching stress per JEP182<sup>(8)</sup>. A highly-reliable diode is used for the high-side device, eliminating high-side drive complexity. Its simplicity minimizes system-related failures, enabling accelerated testing for the desired failure mechanism. It is also designed to measure dynamic  $R_{DS(ON)}$  per JEP173<sup>(9)</sup>.

Traditional silicon qualification testing alone is not a guarantee for reliable application performance because it does not include hard-switching transitions, nor does it test for dynamic  $R_{DS(ON)}$ . Both aspects are very important for the proper operation of all devices in hard-switching applications. We have seen that GaN devices from processes that pass traditional silicon qualification can still overheat and show a decrease in efficiency when run in a in a hard-switched application. However, parts run reliably if the process passes traditional qualification testing plus hard-switching reliability testing<sup>(10)</sup>.

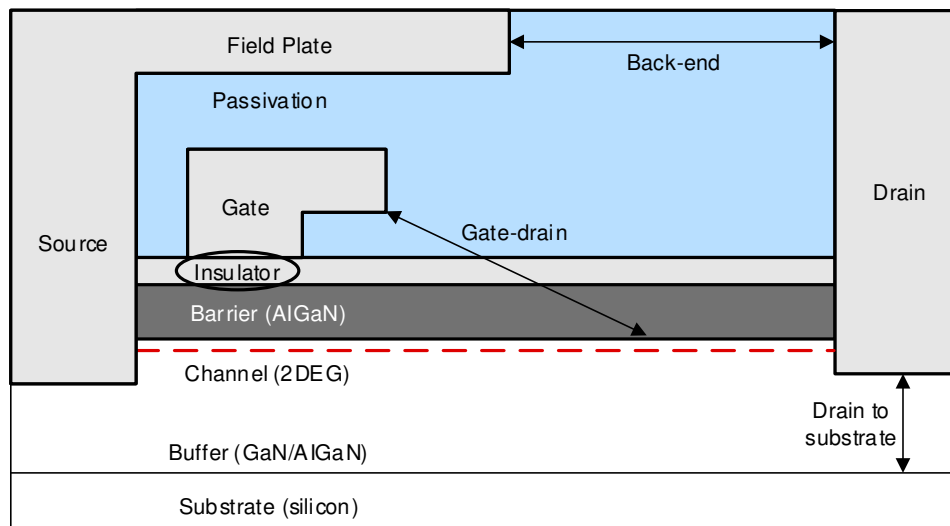
It is often asked whether a device that is robust to hard-switching is also robust for soft-switching applications. This is reasonable thinking because hard-switching creates more hot electrons, which can increase electron trapping and result in higher dynamic  $R_{DS(ON)}$ <sup>(11)</sup>. It was previously shown<sup>(10)</sup> that hard-switching is the more stressful case for TI GaN devices. However, there have been recent literature reports<sup>(12)</sup> that soft-switching can cause higher dynamic  $R_{DS(ON)}$  for some types of devices. Our stress testing confirms that TI GaN devices are reliable for both hard and soft-switching applications and confirms that soft-switching does not cause higher dynamic  $R_{DS(ON)}$  for GaN technology in general.

### 3 Addressing GaN Failure Mechanisms

Failure mechanisms are present in all devices. Reliability engineering consists of making devices robust to failure mechanisms and their resulting failure modes. For GaN devices, the major failure modes are the *increase of leakage currents* and *changes in parameters* such as on-resistance. These can result in a reduction in efficiency or in circuit malfunction. Hard-failure can also occur.

In GaN devices, the primary failure mechanisms are *Time Dependent Breakdown (TDB)*, *hot-carrier degradation*, and *charge trapping*. Time Dependent Breakdown is a well-known phenomenon<sup>(13)</sup> in dielectrics used in silicon processing, and its modeling is treated in JEDEC publications<sup>(14)</sup>. It occurs due to high electric-field and is responsible for increased leakage currents and can lead to hard-failure. Hot-carrier degradation is also well-known in Si MOSFETs, where hot-carrier stress causes defect generation. Hot-carriers are created by hard-switching in power FETs, and have been seen to result in both charge trapping and wearout in GaN FETs<sup>(5, 15)</sup>.

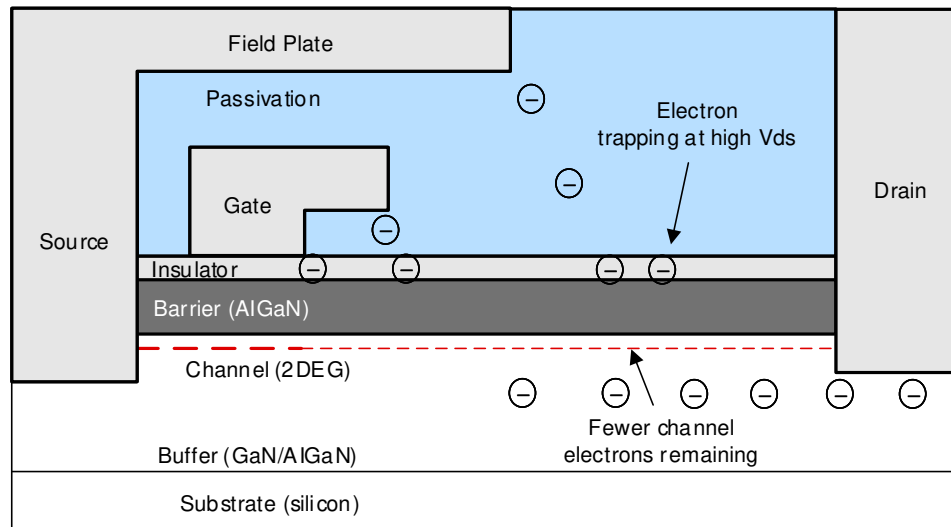
GaN FETs operate with high electric fields in several regions, as shown in [Figure 3-1](#). TI GaN FETs have been engineered for TDB lifetime with the use of special test structures for each of these high-field regions. A model has been built incorporating 1.8 million device hours of testing and shows a low FIT rate of 0.8 FIT with 10 years of continuous application of 480 V and 125°C for the LMG3410R070 product.



**Figure 3-1. Schematic cross-section of the GaN device showing the high-field regions in the device.**

Charge trapping is also a well-known phenomenon in semiconductor devices, and can cause parametric shifts. An important consequence of charge trapping in GaN devices is a shift in the on-resistance,  $R_{DS(ON)}$ <sup>(16)</sup>. Negative trapped charge repels channel electrons, thereby resulting in fewer electrons in the channel, as shown in [Figure 3-2](#).  $R_{DS(ON)}$  increases because the number of electrons in a portion of the channel layer is reduced. Charge can be trapped in the buffer layer, in dielectrics, and at interfaces. Charge trapping can occur due to high drain voltage when the device is off, or from hot electrons when switching. The  $R_{DS(ON)}$  inclusive of charge trapping effects is called dynamic  $R_{DS(ON)}$ . The dynamic nature arises because  $R_{DS(ON)}$  recovers as the trapped charge dissipates or detraps. It is therefore important to evaluate dynamic  $R_{DS(ON)}$  at the timescales of switching cycles. A consequence is that if the detrapping or device on-time is low, there could be more charge buildup. Dynamic  $R_{DS(ON)}$  evaluation at low duty cycle is therefore a good method to validate material quality.

Power devices need to be engineered for stable  $R_{DS(ON)}$ , since they are continually subject to high voltage and hot electron generation while switching. Increases in  $R_{DS(ON)}$ , will decrease efficiency through higher conduction loss. Furthermore, the trap density can increase as the device ages. It is therefore important for dynamic  $R_{DS(ON)}$  to be stable with aging, to prevent excessive self-heating and premature failure.

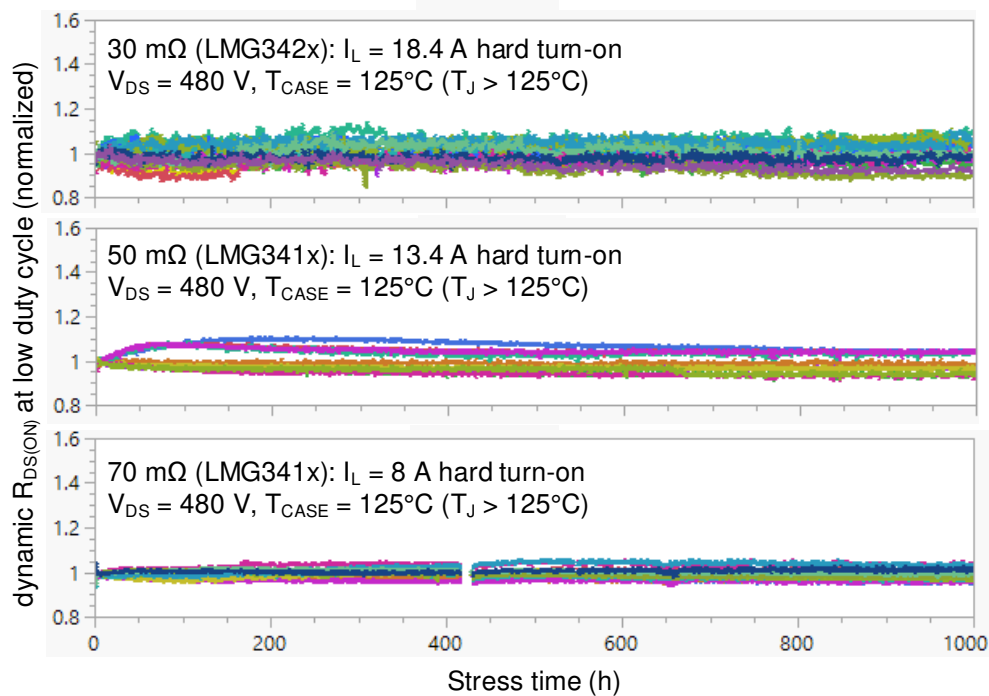


**Figure 3-2. Schematic cross-section of a GaN device shows how trapped electrons can increase  $R_{DS(ON)}$  by reducing the number of electrons in the channel layer**

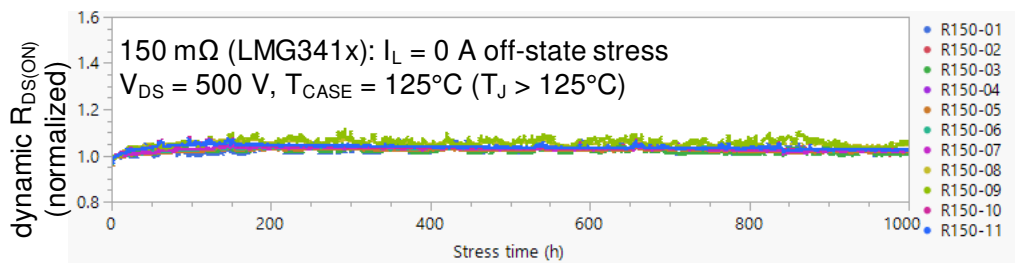
TI GaN products have been engineered for stable dynamic  $R_{DS(ON)}$  with aging. This was achieved through years of in-house material and process engineering. It included ways of growing high-quality GaN crystal, optimizing the dielectric films, and achieving very clean interfaces. We validate dynamic  $R_{DS(ON)}$  lifetime stability by using the test vehicle in [Figure 2-1](#). This is one of the circuits listed in JEP182 for the continuous-switching evaluation of GaN power conversion devices. Hard-switching stress is applied per JEP180 at a current corresponding to the maximum power condition, the maximum recommended  $V_{DS}$  and worst-case junction temperature, for 1000h. Dynamic  $R_{DS(ON)}$  stability with aging is validated through low duty-cycle hard-switching stress. Dynamic  $R_{DS(ON)}$  aging data from products in the LMG34xx family is shown in [Figure 3-3](#). The duty cycle used was about 0.5%, which provides excellent ability to discriminate material quality. Dynamic  $R_{DS(ON)}$  measurement is conducted per JEP173. The high stability of dynamic  $R_{DS(ON)}$  under very low duty cycle for best-practice lifetime stress conditions attests to excellent aging of the material: it demonstrates the lack of new trap creation with aging and validates the long-term stability of dynamic  $R_{DS(ON)}$  under all conditions of operation. To assure manufacturability of material with this quality, we have had a coordinated program to develop in-line electrical tests that are predictive of dynamic  $R_{DS(ON)}$  in application. The excellent dynamic  $R_{DS(ON)}$  stability of our production material has also been verified by others<sup>(16)</sup>.

The reason that low duty cycle provides excellent sensitivity to charge trapping is because the device spends most of its time at high-voltage and the small on-time limits de-trapping<sup>(16, 17)</sup>. This gives the corresponding dynamic  $R_{DS(ON)}$  parameter excellent sensitivity to material quality. The increased sensitivity of dynamic  $R_{DS(ON)}$  to detect trapping helps it pick up less electrically active traps. This is consequential because these latent or nascent defects would become more electrically active as they age and later start affecting dynamic  $R_{DS(ON)}$  for operation at regular duty cycles. Dynamic  $R_{DS(ON)}$  under low duty cycle thereby provides an early detection method for the effects of aging. Stable dynamic  $R_{DS(ON)}$  under low duty cycle stress shows that these latent traps are not a concern.

We also evaluated dynamic  $R_{DS(ON)}$  stability under two other modes of operation in power supplies. First is under prolonged off-state conditions by applying off-state stress at a temperature of 125°C and  $V_{DS} = 500$  V. The dynamic  $R_{DS(ON)}$  is measured in situ every 10 minutes with the results plotted in [Figure 3-4](#), and shows stable behavior with aging. Second is under Dynamic High Temperature Operating Life (DHTOL) operation per JEP180 under both hard and soft-switching operation. The parts had stable efficiency, as described later in section 8, which validates dynamic  $R_{DS(ON)}$  stability. The stable behavior under these conditions further provides assurance that TI GaN technology is natively robust to charge trapping mechanisms.



**Figure 3-3. Dynamic  $R_{DS(ON)}$  is stable under low duty-cycle hard-switching best-practice stress conditions. Parts were run at 15–21 kHz with a duty cycle of about 0.5%. The stability demonstrates lack of new trap creation and attests to the excellent material quality. Dynamic  $R_{DS(ON)}$  is measured per JEP173**



**Figure 3-4. Dynamic  $R_{DS(ON)}$  is stable under off-state high voltage and temperature conditions, providing further assurance that TI GaN is robust to charge trapping mechanisms. The stress was applied using the circuit of Figure 2-1 with  $I_L = 0$  A.**

An important difference between GaN and Si FETs is the mechanism causing breakdown. The drain breakdown voltage of Si power FETs is limited by impact ionization, resulting in their voltage rating being limited by avalanche breakdown. As a result, Silicon power FETs do not have much headroom above their voltage rating for transient events. GaN has avalanche<sup>(18)</sup> capability, but its three-times larger bandgap, allows it to better withstand higher fields without avalanching. The voltage rating of GaN FETs is typically lower than the avalanche limit of the material, giving them transient voltage capability. This aspect allows them to switch through surge without avalanching, as is discussed later.





Finally, it is important to address the effects of current flow at high voltage. Current flows at high voltage during hard-switching in any power device, as explained in reference 5. There are two relevant effects. Firstly, current flow at high voltage creates hot carriers. Their higher energy enables them to scatter into a larger volume, which can result in more charge trapping and cause an increase in dynamic  $R_{DS(ON)}$ . Hot carriers can also cause wear out or degradation due to defect generation. Current flow at high voltage can also exercise safe operating area (SOA) boundaries, for which the part needs lifetime reliability. TI GaN is robust to failure modes arising due to hot carriers. As shown in Figure 3-3, we validate long-term dynamic  $R_{DS(ON)}$  stability at stringent low duty-cycle operation under hot-carrier creating hard switching conditions. The hard-switching lifetime and SOA aspects are discussed later.

## 4 Achieving Lifetime Reliability

TI has engineered GaN products for lifetime reliability through an extensive program, completing over 40 million hours of reliability testing as of November 2020. We realized at an early stage that traditional silicon qualification was not testing for hard switching, nor detecting the GaN-specific failure mode of dynamic  $R_{DS(ON)}$ , so we built our reliability program to address GaN specific needs.

TI GaN products consist of both a GaN chip and a Si IC chip integrated in a Multi-Chip Module (MCM) package using a low-inductance leadframe. Our program ensures reliability of both the individual die and the final product using the methodology of [Figure 1-1](#). These tests are listed in [Table 4-1](#) at both technology and product level. The Si chip integrates the driver and additional protection functions. It is built on an established TI Si platform also used for many silicon IC products. The GaN chip is built using TI's GaN technology platform. Qualification is conducted at multiple levels, first at the technology level on both GaN and Si platforms, then in the final product. The battery of qualification testing includes both traditional and GaN-specific JEDEC testing. It also includes the testing of the product under extreme conditions.

**Table 4-1. The reliability of TI GaN products is ensured both at the technology and product level with qualification, extreme-operation and lifetime testing.**

Intrinsic Reliability	Product Reliability	
Technology-level	Regular operation	Extreme operation
 		
<ul style="list-style-type: none"> <li>• Device reliability (JEDEC JEP122)</li> <li>• Technology qualification (JEDEC JESD47)</li> <li>• Hard-switching lifetime (JEDEC JEP180, JEP182)</li> <li>• <math>dR_{DS(ON)}</math> aging stability (measurement per JEP173)</li> </ul>	<ul style="list-style-type: none"> <li>• JEDEC JESD47, AEC Q100</li> <li>• Product aging stability (Dynamic High Temperature Operating Life, JEP180)</li> </ul>	<ul style="list-style-type: none"> <li>• Lightning Surge                             <ul style="list-style-type: none"> <li>– IEC 61000-4-5</li> <li>– VDE0884-11</li> </ul> </li> <li>• Hard short circuit</li> </ul>

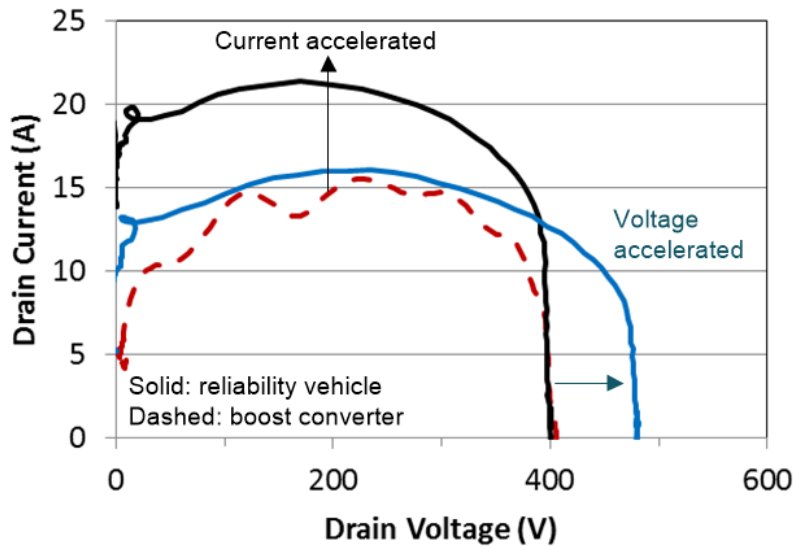
Both technology platforms and the final product are qualified to the JEDEC JESD47 standard. Automotive qualification is per AEC Q-100. For the technology platform, device reliability (TDB) and electromigration are per JEDEC JEP122 and dynamic  $R_{DS(ON)}$  measurements are per JEP173. The hard-switching lifetime and product dynamic high temperature operating life (DHTOL) are per JEDEC JEP180 and JEP182. The product is also tested under extreme conditions for surge and short-circuit robustness.



## 5 Achieving Lifetime Switching

Power semiconductor devices need to be engineered to withstand hot-carrier effects occurring during switching. Tests used for Si FET reliability and robustness are not applicable to GaN FETs due to structural and material differences. For example the Hot Carrier Injection (HCI) test for lateral power FETs is not useful because the GaN FET has an electrically blocking buffer, and the Unclamped Inductive Switching (UIS) test could cause damage. JEP180 addresses this aspect, and in this section, we will show how TI GaN has been validated to be reliable for switching applications.

We apply accelerated hard-switching stress, per JEP180, using the continuous switching test-vehicle circuit of [Figure 2-1](#) (per JEP182). [Figure 5-1](#) shows how switching stress may be accelerated vs. that experienced under normal operation. The figure shows the switching locus curve or turn-on trajectory of a boost converter (dashed curve) operating at a bus voltage of 400 V and an inductor current of 5 A. The solid loci are from the test-vehicle circuit in [Figure 2-1](#), at bus voltages and inductor currents of 400 V, 15 A and 480 V, 5 A showing current and voltage acceleration respectively.



**Figure 5-1. The test-vehicle circuit in [Figure 2-1](#) is used to apply accelerated hard switching stress, illustrated by the switching locus curves.**

We ran accelerated lifetime testing for voltage, current, temperature and frequency and generated a model as described in reference [19](#). Our approach calculates the switching stress by integrating the switching waveform while applying the voltage and current acceleration factors. This allows the complexity of the switching transition to be addressed. It enables stress to be applied using a suitable test-vehicle circuit, and for the switching lifetime to be calculated for broad application use as shown in [Figure 5-2](#).

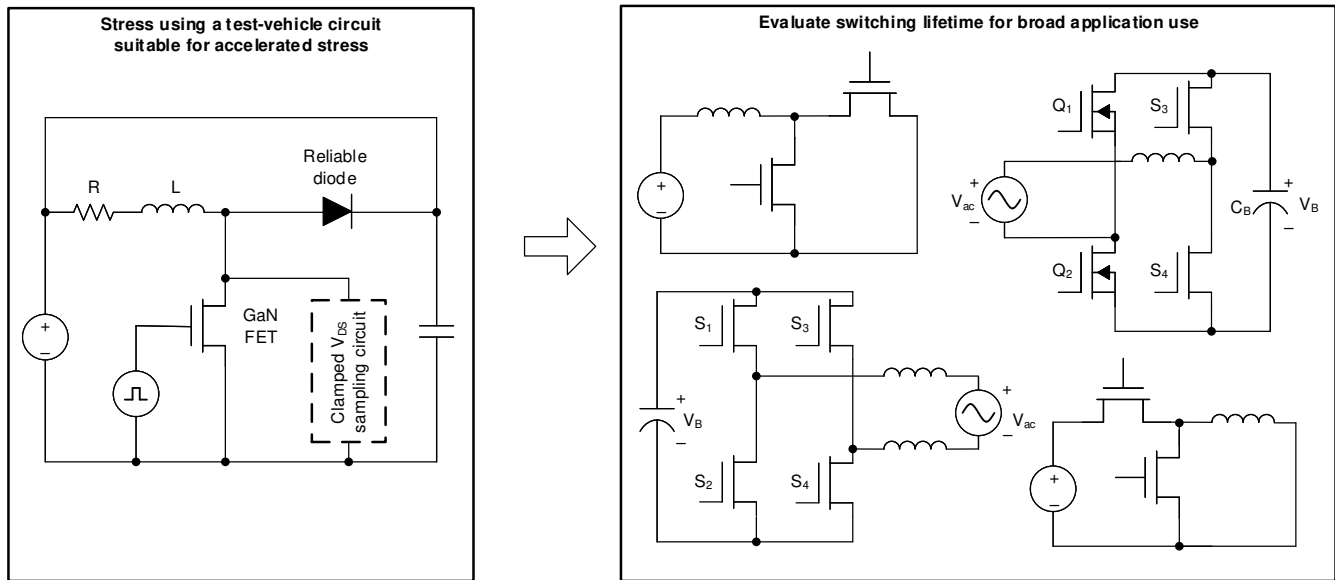


Figure 5-2. Our switching lifetime methodology allows for accelerated switching stress to be applied by a test-vehicle circuit, and the switching lifetime to be calculated for broad application usage.

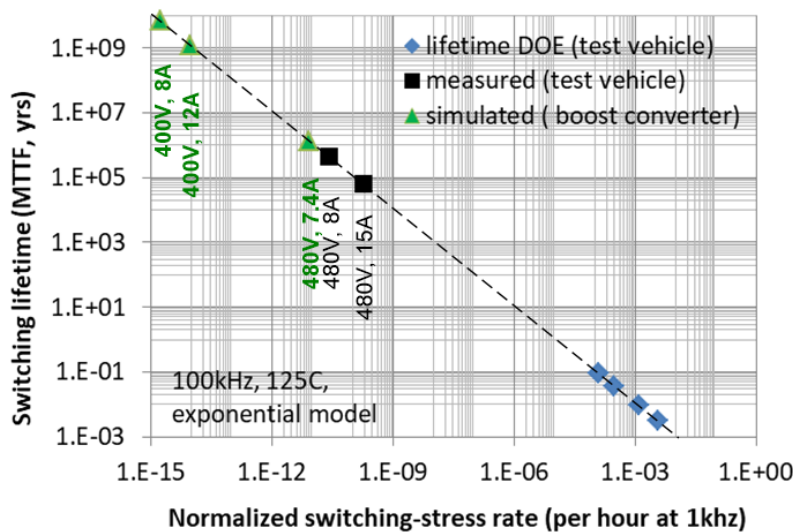


Figure 5-3. Switching lifetime MTTF calculation from both measured and simulated waveforms (black and green points). The blue points represent the lifetime run of DOE. The device is very reliable for hard switching.

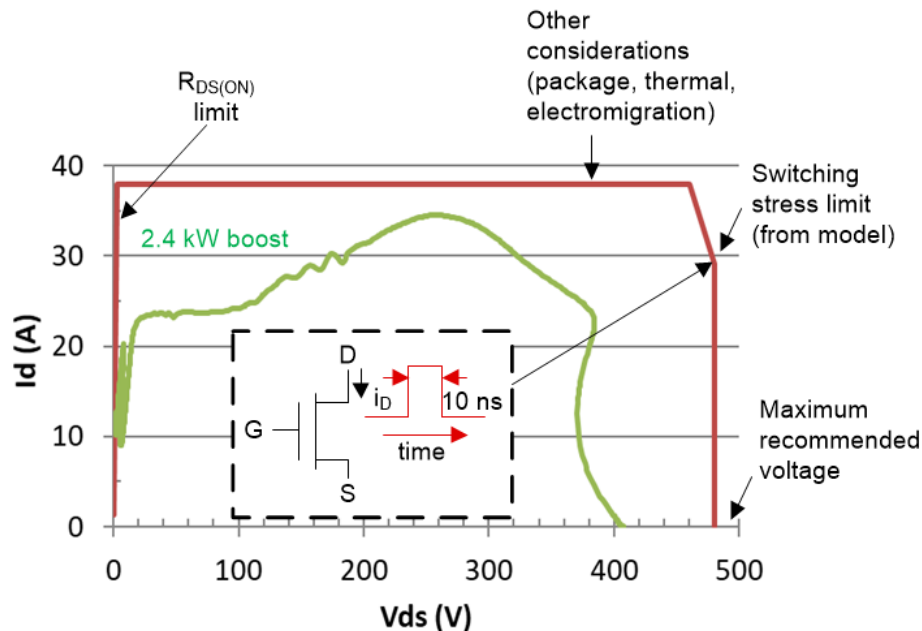
The model is used to calculate a normalized switching stress rate as shown in Figure 5-3, from which the lifetime for any given application operation can be determined. Both measured and simulated waveforms can be used, providing tremendous flexibility. The model can also be used in the calculation of time-varying stress, for example, for a PFC with AC line cycle as shown in reference 19. A Mean Time to Failure (MTTF) of  $8.46 \times 10^9$  yrs was calculated for a LMG3410R070 (70 mΩ) Integrated GaN FET Power Stage switching at 100 kHz (100 V/ns), with 400 V output, 8 A RMS inductor current in Continuous Conduction Mode (CCM). With 230 V RMS AC line input (1.84 kW). The high MTTF assures that there will be no intrinsic failure due to hot-electron wear out from hard-switching stress during regular operation.

## 6 Achieving Reliable Design

For the reliable operation of a power converter, the device needs to stay within certain voltage and current ranges. The designer looks to the Safe Operating Area (SOA) curve<sup>(20)</sup> for the limits and assumes that designs within SOA limits will be reliable for long-term operation. Measurements for traditional SOA curves are conducted using single current-pulses with the FET biased in saturation. Pulse widths used are typically longer than 100 μs and the measured boundary is typically derated by 30–35% to provide extra margin.

Since traditional SOA curves are empirically determined, it is not clear how they will guide the reliable design of modern power supplies. Fast power FETs can switch in less than 10 ns, but need to carry higher switching current due to the fast slew rate<sup>(5)</sup>. Traditional SOA curves do not take into account wearout and the resulting lifetime implications due to repetitive switching at these conditions.

The switching SOA curve can guide the reliable design of modern power supplies by use of the switching stress model to calculate the switching stress limit. We have applied the model to generate the SOA curve in Figure 6-1 shown for the LMG3410R050. This switching stress boundary is calculated for 100-kHz operation with an ideal 10 ns drain-current pulse, illustrated in the inset, at each fixed value of  $V_{DS}$ , where the drain current is defined as the current entering the drain terminal. The other boundaries of the curve are determined by different considerations. The figure also shows the switching locus curve of a hard-switched turn-on transition corresponding to 2.4 kW boost operation and switching time of 10 ns. Since the switching trajectory fits within the boundary, the part will operate reliably at this condition. In addition, there is margin, since the time at high voltage, where most wear out occurs, will be lower than 10 ns.



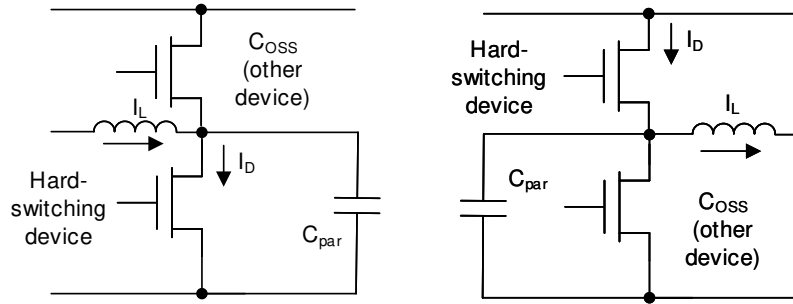
**Figure 6-1. SOA curve with use of switching lifetime model to calculate the maximum switching stress limit. This boundary is calculated for a 10-ns switching pulse and 100-kHz operation. Applications with switching locus curves within the boundary will operate reliably. The use of a linear  $V_{DS}$  scale provides better resolution at high voltage.**

If either a measured or simulated switching locus curve is not available, the peak drain current during switching may be estimated using Equation 1. The peak drain current is calculated by adding the switched node capacitive charging current to the peak inductor current of a boost or buck converter at the time of FET turn-on of the hard-switching device:

$$i_D = I_L + C_{SW\_node} \times dv_{DS}/dt \tag{1}$$

The drain slew rate for calculating the peak current ( $I_{Dpeak}$ ) is estimated between 70 percent and 30 percent of the bus voltage and the switched node capacitance ( $C_{SW\_node}$ ) is estimated as the sum of the overlap

capacitance of the PCB ( $C_{par}$ ) and output capacitance  $C_{OSS}$  of the other GaN device in the half-bridge. The method is applicable for both buck and boost topologies, as shown in Figure 6-2.



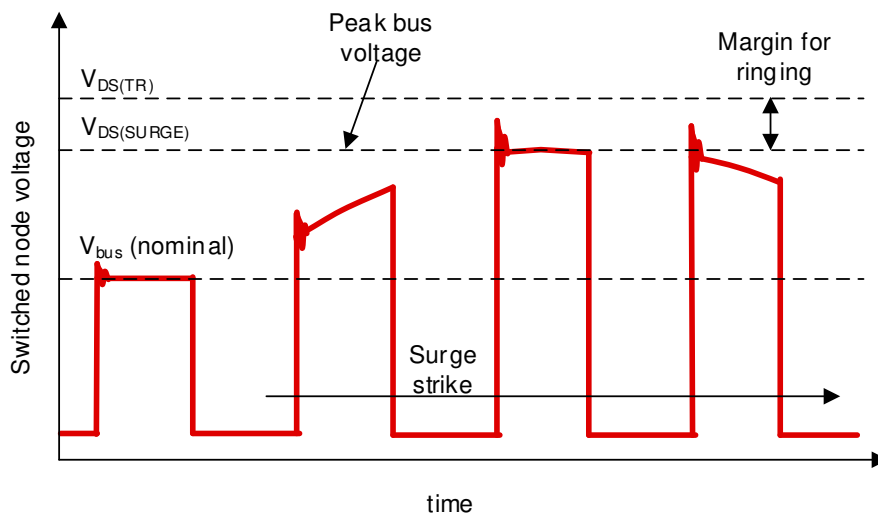
**Figure 6-2. The calculation of drain current while switching (Equation 1) is valid for both boost and buck topologies, for the hard-switching device. The capacitance at the switched node is the sum of the PCB overlap capacitance and the  $C_{OSS}$  of the other device in the half-bridge.**

## 7 Achieving Surge Robustness

The association of avalanche rating with surge robustness arises because the drain breakdown voltage of Si power FETs is typically limited by impact ionization or avalanche breakdown. When a power-line surge strikes, the FET breaks down by avalanche as its drain voltage exceeds the breakdown voltage. Silicon FETs therefore provide surge robustness via avalanche capability.

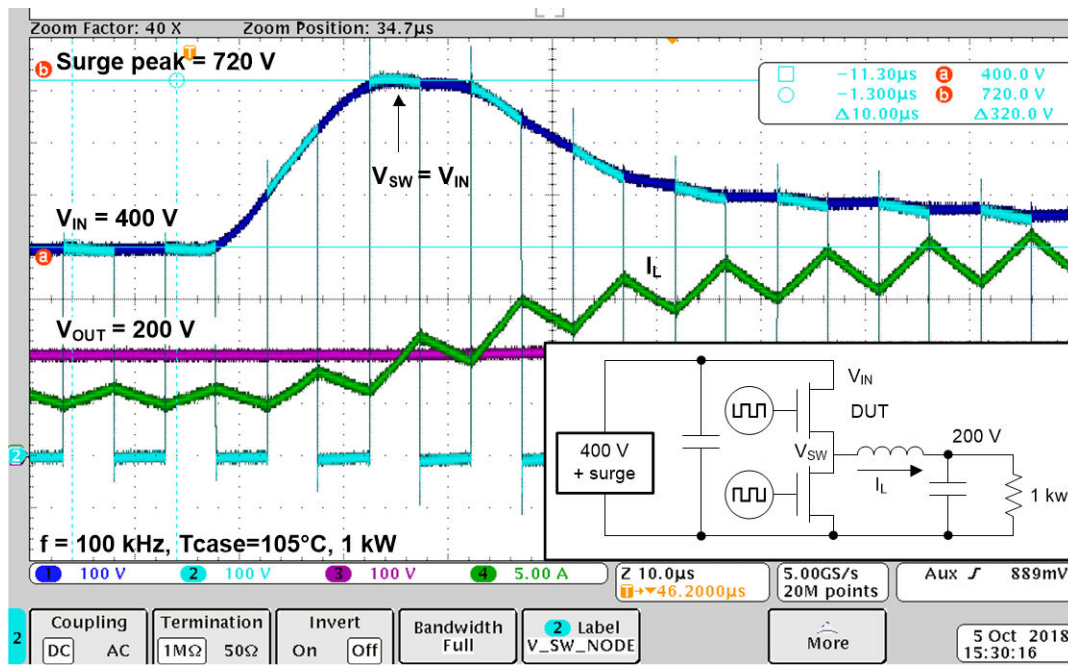
GaN has much lower impact ionization coefficients than Si<sup>(21, 22)</sup> as a result of its superior high-field withstand properties. The voltage rating of GaN FETs is not limited by avalanche, and there is headroom above it for transient events. As a result, GaN FETs have the ability to switch through surge events. GaN FETs are surge robust because they have transient overvoltage capability.

The data sheet parameter,  $V_{DS(SURGE)}$ , was introduced to quantify the peak bus voltage that may be applied to the GaN FET when actively switching the load current during a surge strike<sup>(23, 24)</sup>. This definition provides a simple specification for surge-robust power supply design.  $V_{DS(SURGE)}$  supplements the  $V_{DS(TR)}$  rating already present in the data sheets of several manufacturers.  $V_{DS(TR)}$  is typically measured with the device off, and therefore quantifies the margin available for ringing (for example, with the channel off). Figure 7-1 shows these parameters.



**Figure 7-1.  $V_{DS(SURGE)}$  is the peak bus voltage the GaN FET can actively switch through during surge.  $V_{DS(TR)}$  provides extra margin for ringing.**

TI GaN FETs are validated for  $V_{DS(SURGE)}$  by applying fifty strikes per the IEC 61000-4-5 surge standard<sup>(25)</sup> to a half-bridge delivering power under actual use hard-switching conditions. A detailed description of the validation of the LMG3410R070 is provided in reference 24. Fifty strikes per VDE 0884-11<sup>(26)</sup> were applied to a half bridge operating at  $V_{DS} = 400$  V, 100 kHz, 50% duty cycle, and delivering 1 kW of power with a case temperature of the hard-switching device at 105°C. The peak bus voltage at the devices was set to 720 V. The schematic and waveforms are shown in Figure 7-2. The figure shows the bus voltage surging to 720 V with application of the strike. The switched node waveform is overlaid on the input waveform to show the switching transitions. An increase in the inductor current from 5 A to 20 A is also seen, further validating the robustness. The use of a half-bridge allows the validation of all modes of device operation under both voltage and current surges: hard switching, soft switching, blocking, and third quadrant operation and its hard-commutation turn-off. The test does not cause hard-fail or efficiency degradation.



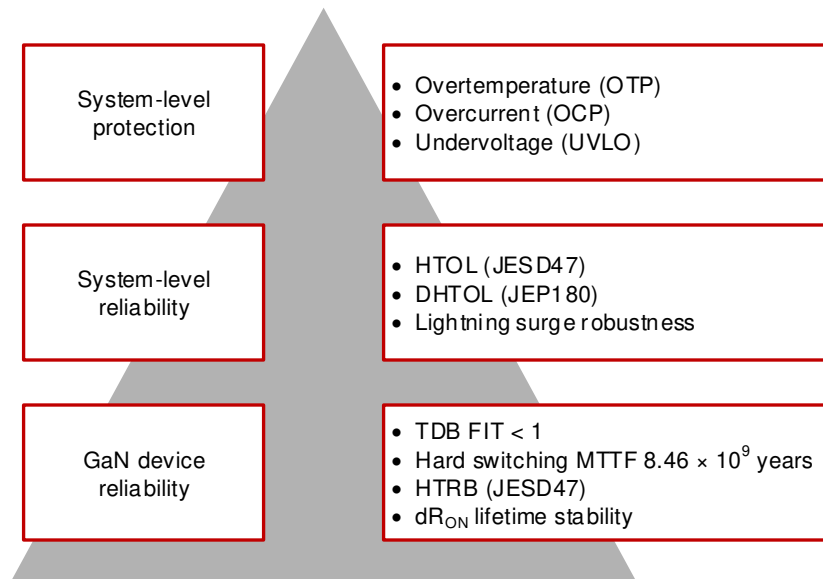
**Figure 7-2. Surge waveforms, showing the test point parameters of the schematic (inset). The switched node waveform is overlaid on the input waveform to show switching through the surge strike.**

The surge-voltage specification,  $V_{DS(SURGE)}$ , makes it straightforward to design a robust power supply with GaN. This is because the schematic for a surge generator is specified in the standard and can be implemented in a simulator. This allows component values to be selected such that the bus voltage at the device remains below 720 V during surge. Our simulations showed that the application of a 4-kV surge strike to the input of a power supply resulted in a peak bus voltage of only 570 V at the GaN FET. Four kV is the highest defined voltage of the IEC surge standard. This shows that it is straightforward to limit the peak surge voltage at the FET with margin, even for severe surge conditions.

The overvoltage capability of GaN is advantageous to the avalanche capability of Si. It allows the power supply to not drop the load and provide a robust power solution. Overvoltage ability also provides more protection margin than avalanche over the system lifetime. This is because FETs do not have the avalanche capability to absorb much energy or offer much clamping, therefore the clamping circuitry needs to bear the brunt of the surge. Degradation of the clamping circuitry, for example, MOVs over their lifetime will expose an avalanching FET to higher levels of surge voltage and increase the risk of failure.

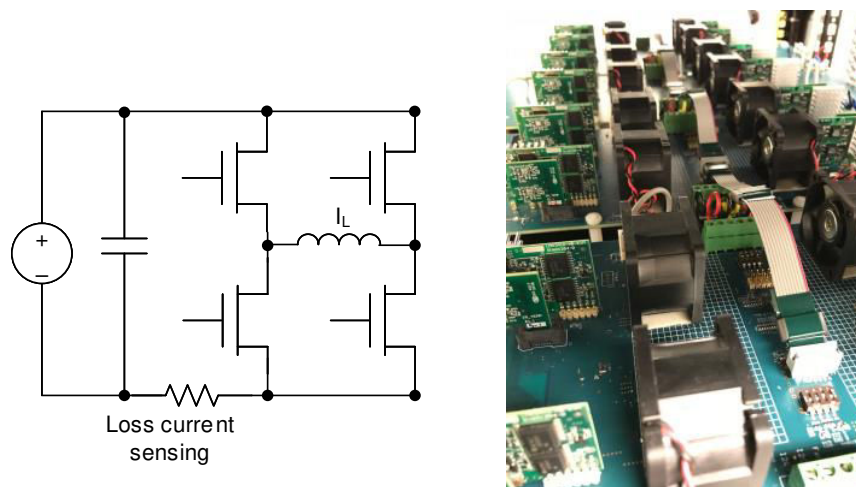
## 8 System-Level Reliability and Protection

Two important aspects of TI GaN products are their reliable operation in power supplies and the built-in protection functions that can improve system-level reliability. These aspects are built upon a reliable GaN device foundation, shown in Figure 8-1. The system-level protections include overtemperature and overcurrent protection, and undervoltage lockout. In addition, the low-inductance leadframe minimizes ringing and related voltage overstress, thereby improving reliability.



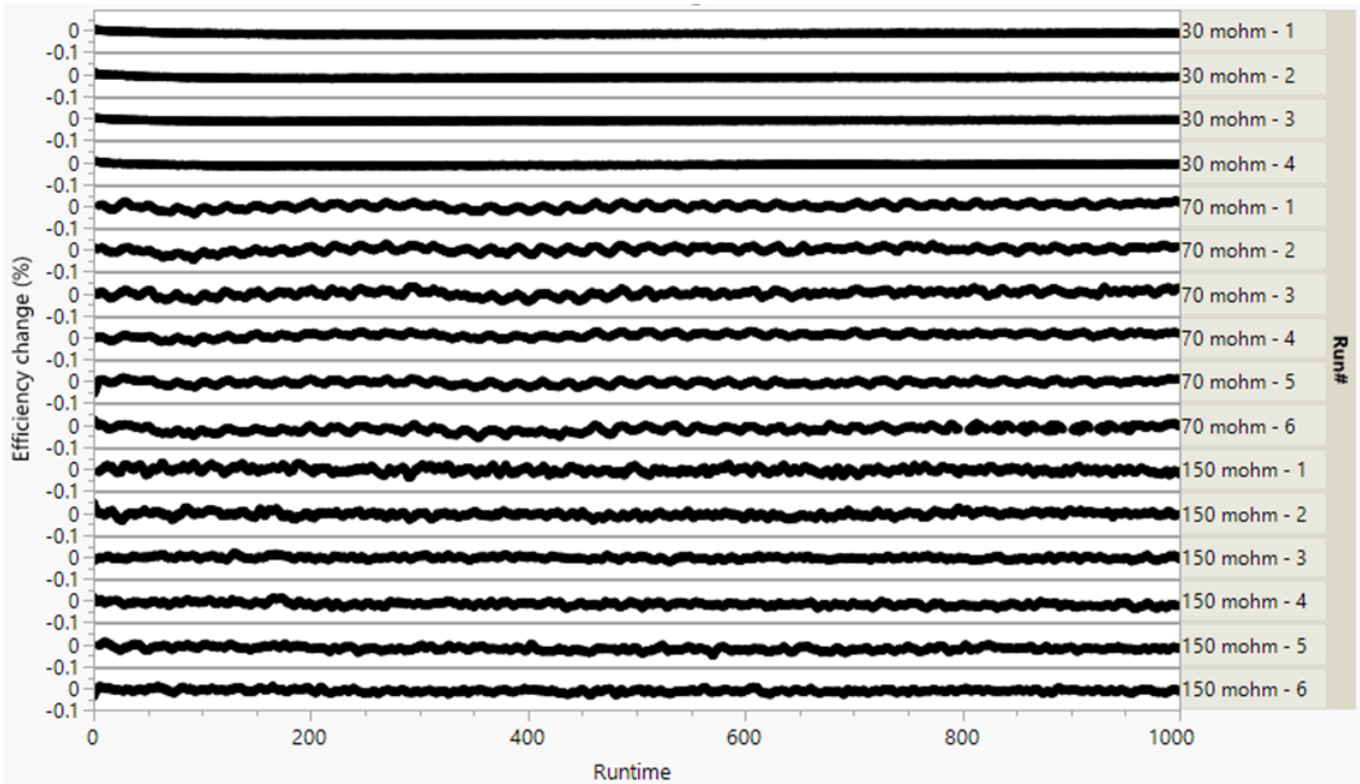
**Figure 8-1. System-level reliability and protections of TI GaN products are built on a solid device foundation.**

System-level reliability is validated through the JESD47 High Temperature Operating Life (HTOL) test, the JEP180 Dynamic (DHTOL) test, and the lightning surge test described in Section 7. We run the JESD47 HTOL test with 3 lots  $\times$  77 parts of the product at maximum recommended voltages and temperatures in HTOL boards. Hard-switching under the conditions of power conversion applications is not feasible in socketed HTOL boards, so the HTOL test is designed to exercise both the off-state and functional-switching reliability of the MCM product. Hard-switching under the conditions of power conversion applications is performed per the JEP180 DHTOL testing guideline using half-bridge cards in an H-bridge configuration. The half-bridge cards are based upon our customer Evaluation Module (EVM), and are inserted into an array of H-bridge motherboards, as shown in Figure 8-2.



**Figure 8-2. Dynamic HTOL (DHTOL) is run using an H-bridge cell comprising two half-bridge cards. Both hard and soft-switching stress is applied.**

The cards are stressed using JEP180 best-practice conditions of maximum recommended voltage, temperature, and power levels and run for 1000 h with parts stressed under both hard- and soft-switching conditions. The test validates both hard and soft-switching reliability by applying system-level stress to the part. It also assures there are no failures from other modes like third quadrant operation and hard-commutation. It further checks the robustness of interactions, for example, with the other die in the MCM, the other half-bridge GaN part, or with other components typically used in power supplies. The parts show stable efficiency and they run without fail, as shown in Figure 8-3, which shows DHTOL results on 32 half-bridge cards (64 parts) from the LMG34xx product family from multiple fabrication lots. The stress conditions are listed in the figure caption. Each trellis in Figure 8-3 shows the efficiency change of one H-bridge cell (4 parts), calculated from the loss current needed to power the cell. The efficiency remained within 0.1% of its initial value, demonstrating the good system-level reliability of TI GaN products. The result provides confidence that parts will operate stably as they age. This is due to their excellent dynamic  $R_{DS(ON)}$  stability, previously shown under conditions of both hard switching and off-state stress. The DHTOL test also validates that the switching transition remains clean, without shoot-through effects at high slew rates of 100 V/ns.



**Figure 8-3. Dynamic HTOL (DHTOL) results on LMG3410 TI GaN parts run at 480V/125C, 150 kHz, 100 V/ns slew rate and maximum-power stress conditions for 1000h. Power levels used were: 3.8 kW for 30 mΩ, 1.9 kW for 50 mΩ, 1.4 kW for 150 mΩ. Parts run stably without failure, and efficiency remained within 0.1%. demonstrating good in-system reliability.**



## 9 Automotive

TI's new AEC Q-100 rated GaN FETs can help reduce the size of electric vehicle (EV) onboard chargers and DC/DC converters by as much as 50% compared to existing Si or SiC solutions, offering electric vehicles an extended battery range with increased system reliability at a lower design cost.

In addition to the GaN-specific testing described in the prior sections of this white paper, TI's automotive GaN products are subjected to AEC Q100 testing. A primary difference between AEC Q100 and JESD47 qualification is that the Q100 product is qualified based upon the temperature grade<sup>(27)</sup>. Our initial automotive parts will be released at grade 1. TI's methodology is also able to evaluate products for a range of operating conditions, given a mission profile, for both switching stress<sup>(19)</sup> and TDB failure mechanisms.

## 10 Conclusion

Texas Instruments has longstanding expertise with the qualification of semiconductor products, which is brought to bear on qualifying GaN. We have additionally developed new methodologies and supported standardization efforts of the GaN industry. Our approach builds upon well-established silicon standards to consider GaN product operation under both normal and extreme conditions.

TI GaN products have been engineered for lifetime reliability by addressing the failure mechanisms and test considerations of GaN. TI GaN is robust to Time-Dependent Breakdown (TDB), with a FIT rate less than one, is robust to hot-electron wearout from hard-switching with MTTF over a billion years for typical operation, has stable dynamic  $R_{DS(ON)}$  with aging, and operates reliably in power-supply systems. In addition, TI GaN hard-switches through lightning surge events and has many system-level protection features such as overcurrent and temperature protection, and undervoltage lockout protection.

To learn more about TI's GaN solutions, see [www.ti.com/GaN](http://www.ti.com/GaN).

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