Microwave Journal

eBook

Improving RF GaN Success

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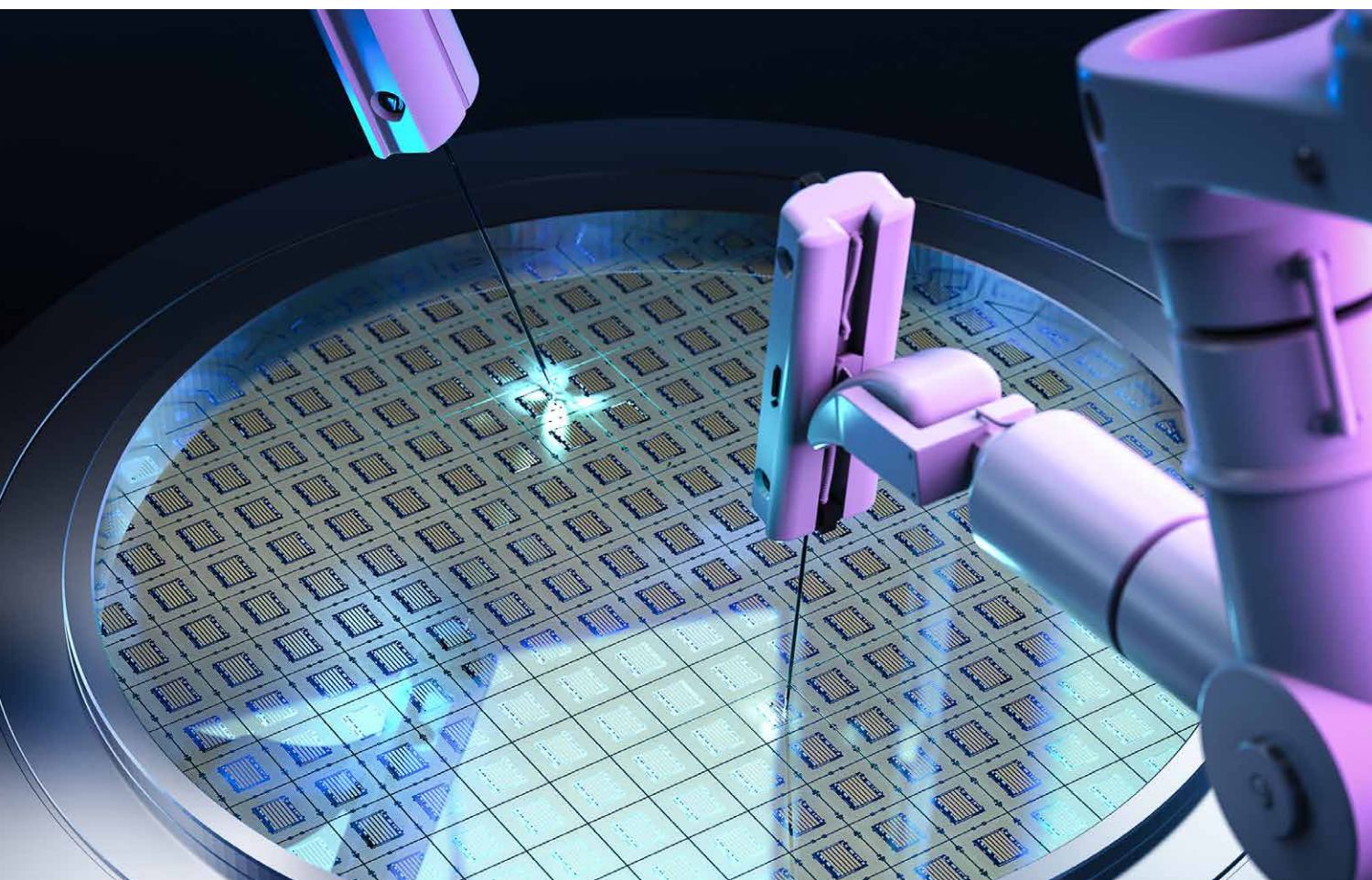

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Introduction

Improving RF GaN Success

Designing a semiconductor component is not easy: the myriad specifications, simulating performance, the cycle time through the wafer fab, packaging, designing and building the evaluation board, testing the circuit — all contributing to the total cost of development. That's why first-pass design success is the holy grail of IC design, even for simpler board designs that use discrete devices.

With GaN being widely adopted for military and commercial systems, the RFIC industry has focused on the device physics, modeling and simulations tools to enable first-pass success with GaN devices. This eBook sponsored by Wolfspeed explores the topic, compiling several recent articles published by Microwave Journal.

The lead article, "Verification of Wireless Systems," written by Cadence Design Systems, describes the simulation flow from system-level requirements to the "test benches" used to test specific parameters. Regression tools can automate the verification process to assure all requirements have been met, helping speed the design process and reducing the likelihood of errors.

"RF/Microwave EDA: Circuit to System Design Challenges and Solutions," from Keysight Technologies, discusses three electronic design automation (EDA) challenges when designing RFICs, multi-chip modules and systems: 1) multilayer and multi-technology integration, 2) electromagnetic (EM) effects on circuit simulation and 3) EM effects on system simulation. As most designs require multiple tools for simulation, standardizing the data interfaces among tools speeds the process and reduces the opportunity for errors.

Moving from simulation to GaN circuit design, Wolfspeed's article "A Dive Into Integrated PA Topologies for 5G mMIMO" describes using GaN power transistors in the popular Doherty power amplifier (PA) architecture. The authors focus on mMIMO PAs, which require small size because of the number of channels and antenna elements. The size constraints favor fully integrated Doherty transistors, and the authors assess the tradeoffs leading to an integrated design.

A second Doherty design article, "Improving Linearity of a Doherty Power Amplifier with a Dual-Bias Structure" contributed by authors at Hangzhou Dianzi University and the Chinese Academy of Sciences, uses a Wolfspeed GaN HEMT in a 3.4 to 3.6 GHz PA design. The design uses a dual-bias network to increase video bandwidth and reduce the GaN memory effect. Using digital predistortion, a prototype PA amplifying a 20 MHz LTE signal with a PAPR of 7.1 dB achieved a measured ACLR better than −46 dBc.

The performance of a semiconductor component doesn't just depend on the semiconductor technology; the off-chip passive components can enhance or degrade the performance. "Using Off-Chip Passive Components to Maximize GaN Performance & Reduce Cost," contributed by AVX, explores several off-chip passive component technologies that can be used to optimize GaN circuits, by providing impedance matching, bias filtering, DC blocking and thermal control. The surface-mount heat pipes are particularly interesting and useful. They can improve the heat flow from an active device and offer high thermal conductivity with reduced parasitic capacitance, higher insulation resistance and high breakdown voltage.

The final article in the eBook, also contributed by Wolfspeed, discusses the foundation for successful power amplifier designs: device models that enable accurate simulation of circuit performance. Like any semiconductor technology, GaN has unique characteristics. Its higher power density, self-heating and resulting thermal effects must be modeled, as well as its nonlinear parameters that are dependent on the signal level. The article lists six requirements for a device model to accurately simulate the small- and large-signal behavior of a GaN circuit.

Gary Lerude, Microwave Journal *Editor*

Verification of Wireless Systems

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For smartphones, new technologies like 5G provide faster access to the internet while on the move, as well as more bandwidth, smaller form factors and longer battery life. To give consumers more goodies, designers must integrate more functionality into their products. In many applications, this problem is solved by using higher levels of integration, that is, using SoC design to achieve higher performance. Unfortunately, it is difficult to realize 5G systems just using SoC designs. To achieve the levels of performance required for 5G designs, heterogeneous designs that integrate multiple technologies—such as silicon, GaAs, GaN—are needed.

Looking at the evolution of cell phone technologies over the long durée, we can see the trend from board-level products realized with discrete components to highly integrated products using SoC and RF modules (see ***Figure 1***). This product evolution requires significant changes in the design methodology. In early designs, the designers could focus on RF block-level design because system-level integration was performed at the board-level of the design. However, when designing for 5G, the level of integration and the complexity of the functionality means that designers need to up their games—the effort required to verify their designs has increased significantly.

The challenge is how to perform complete design verification without impacting time to market. Digital designers have evolved sophisticated methodologies that enable comprehensive verification of their designs without clobbering the time to market for their products. Sadly, until cell-based design has been enabled for custom IC design, this methodology to reduce verification time can't be applied directly to the mixed-signal and RF components in a design. Luckily, this methodology can be adapted for mixed-signal and RF design in three steps:

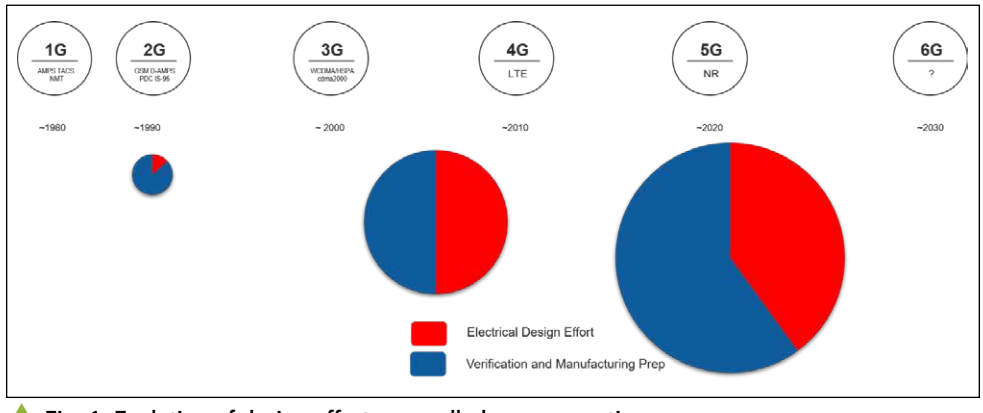

Fig. 1 Evolution of design effort over cell phone generations.

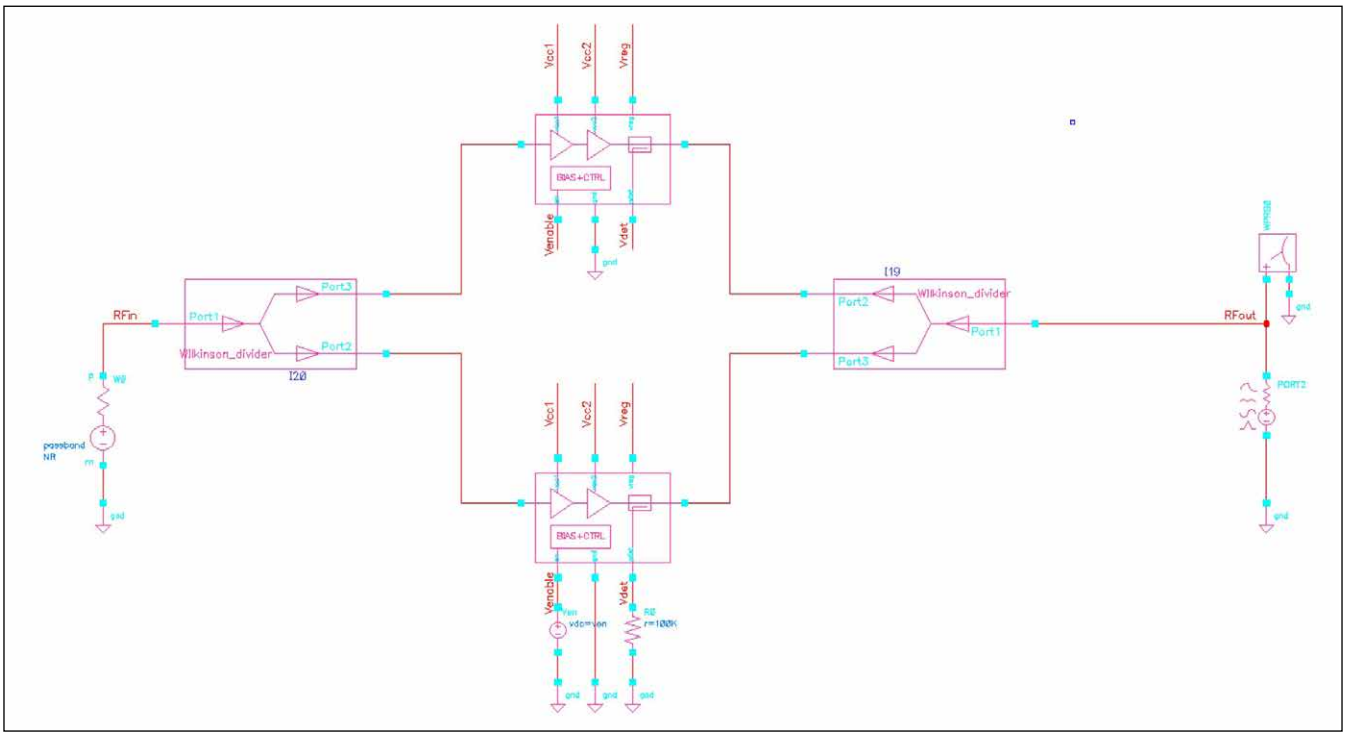

Fig. 2 5G NR wireless testbench for a power amplifier.

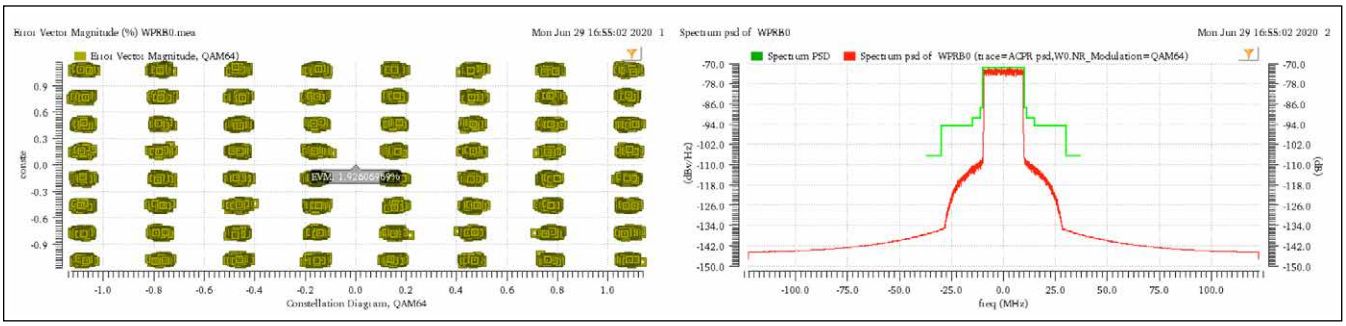

Fig. 3 Results of system-level simulation.

1. Perform system-level simulation. To identify issues as early in the design process as possible, we need to move the system-level measurements into the IC design environment, making 5G sources available to RFIC designers to enable verification.
2. Automate RF verification. Automation has been used extensively by digital designers to overcome the challenges of design verification. We can borrow this concept, enabling the methodology by building on the existing capabilities of the Virtuoso ADE Product Suite. Since most designers are experienced with this product, this minimizes the learning curve.
3. Automate RF regression testing. Verification planning is a systematic approach for defining what needs to be verified and how to verify it.

PERFORMING SYSTEM-LEVEL SIMULATION

Traditionally, RF designers must export their designs to system-level simulators since complex stimulus is required to verify system-level compliance. Even if the stimulus can be imported from the system-level simulator to perform envelope-following analysis, it is a herculean task to set up the simulation to achieve the high accuracy needed for system-level simulation. This approach to verification of passing the problem "over the wall" is known to cause issues, as it is highly dependent on good communications between the parties to achieve design closure.

An alternative approach would be to verify that a design is compliant to standards as part of the block-level verification process. However, for circuit designers to perform system-level simulations, a change in the use model is required. A designer usually sets up the testbench to characterize the design (see ***Figure 2***). Now, designers must understand the system-level measurements to set up the simulations, which can be challenging. The solution is to change the use model so that designers define the measurement they want to perform instead of setting up simulations.

By allowing designers to focus on the measurement they want to perform, such as selecting the channel number or modulation type, productivity can be significantly improved. Once the measurement is defined, the simulation can be set up automatically to optimize

the accuracy. Designers need to perform multiple measurements, including error vector magnitude (EVM), bit error rate, and adjacent channel power ratio (ACPR). Another challenge: performing system-level simulations at the transistor level can be time consuming. As a result, the solution must include the ability to perform fast envelope analysis, which was developed to accelerate system-level simulation time. With fast envelope analysis, designers can confirm that their designs are compliant to standards in a reasonable time. ***Figure 3*** shows the constellation plot used to calculate the EVM and the spectrum with the spectral mask used to calculate ACPR.

To summarize this first step, circuit designers test designs for compliance to standards using existing design tools. The result is less effort for system-level verification since the design is correct by construction.

AUTOMATING RF VERIFICATION

Step two of the methodology is to gather all the tests required to assure compliance so they can be run. Previously, designers would perform this task manually, then compile the results into spreadsheets. This manual process requires significant effort from the designer to maintain the spreadsheet throughout the project. Since the data entry is manual, it is prone to error when generating the document for process corners, across operating modes, etc. If this methodology is performed manually, there is significant risk to both the product development time and potential design issues being missed by the verification. Compared to digital design verification, where there are daily regression runs, this approach to design verification is problematic.

Once automated, the tool then can be used to manage the verification. All the individual tests being performed are gathered into a single regression test for the block. Each measurement includes a specification, the measurement value after the simulation and a judgment whether the result passes or fails—that is, if the measurement is compliant.

For example, there might be separate testbenches for the power dissipation in different modes in addition to the system-level measurements. All the tests required can be captured in a single cell view (see ***Figure 4***). The box highlighted in red shows another useful feature for automating verification across multiple modes of operation, which is often needed. In the figure, the performance with different modulations is being tested.

However, simulating and verifying blocks is useful but not sufficient. Designers need a simulation controller to automate the regression test of their designs once the verification test has been defined.

To summarize, by collecting the wireless testbenches to create automated regression tests for a design, designers can perform daily regression tests to assure the blocks will meet the system-level requirements without impacting the design schedule. The designer can click a button to kick off the regression test and come back when it is complete, to check the results and minimize the impact of verification on time to market.

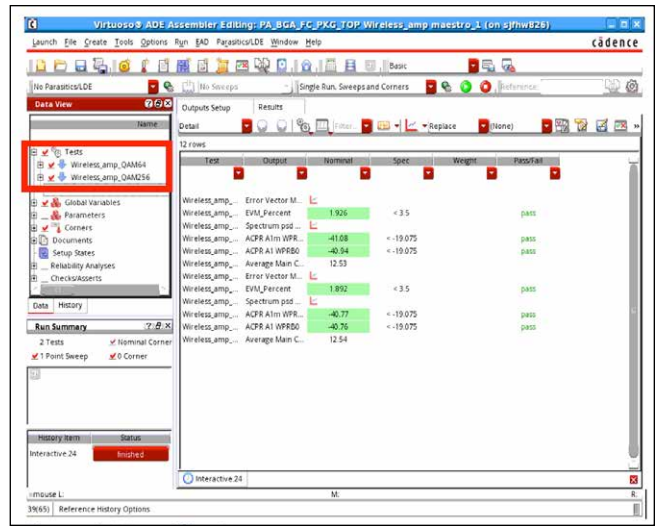

Fig. 4 Power amplifier verification.

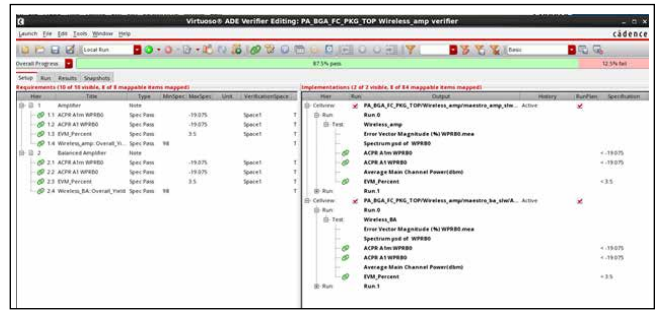

Fig. 5 Power amplifier regression testing.

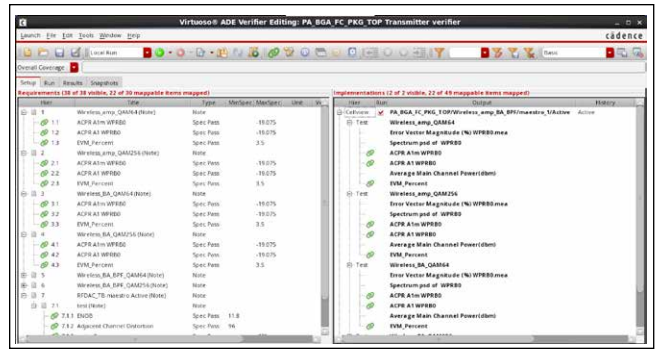

Fig. 6 RF transceiver showing testbench mapping.

AUTOMATING RF REGRESSION TESTING

The final step in this methodology is verification planning. In step two, we looked at how the verification process could be automated; in this step, we look at how to map the system-level designer's requirement for a block to the verification test.

Using the system-level requirements to drive the verification means nothing is missing in the verification test. ***Figure 5*** shows how the system-level requirements can be mapped to the verification tests discussed previously. The left panel captures the requirements from the system-level designers, and the right panel describes the implementation and the tests to verify each of the requirements. Sometime, one requirement can require

multiple tests to verify. Up to this point, we have been discussing verification of a single block; however, real designs have many blocks.

Figure 6 provides a cell view showing a transmitter chain including a power amplifier, the power amplifier integrated into a balanced amplifier and other blocks such as an up-converter and the baseband digital-to-analog converter used to generate the transmission signals. For each system-level requirement, testbenches are required for the mapping, shown by the green chain link. Mapping assures no holes in the regression test used for verification.

Once the regression suite has been created, the next step is to automate the regression process. While this example shows a system-level verification of an RF transmitter, the basic methodology is generic. For example, the requirements could be from a product datasheet for a design. The solution also supports automating the regression suite, since running the test is as easy as pushing a button.

CONCLUSION

To summarize, just verifying a parameter is not enough. Designers need to be able to plan, that is, link from the system-level requirements to the various testbenches designers create to verify the design is compliant with the standard it must support. These simulations can be automated, enabling regular regression runs to be performed.■

RF/Microwave EDA: Circuit to System Design Challenges and Solutions

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Industry trends toward higher frequencies and more complex integrated systems require new design techniques and more extensive simulation.

Can you remember a time when RF standards drove such a rapid rate of change? In transitioning from 4G to 5G, frequencies have increased 40x—700 to 2600 MHz and 28 to 40 GHz—while automotive radar frequency bands have increased from 24 to 77 GHz. As frequencies increase, the density and complexity of system integration also increase, specifically with the integration of phased array antennas.

Trends toward higher frequencies have significant consequences for RF and microwave component and system design. Existing design flows require new techniques to keep pace with the design challenges in the 5G, automotive radar and aerospace/defense markets. Three of the top electronic design automation (EDA) challenges for designers of RF and microwave circuits, modules and systems are:

- Multilayer, multi-technology integration
- Electromagnetic (EM) effects on circuit simulation
- EM effects on system simulation.

MULTILAYER, MULTI-TECHNOLOGY INTEGRATION

Increasing RF frequencies, RF coupling and integration densities create challenges for designers. They must correctly lay out 3D avoidance-route, multi-technology RF modules to connect RFICs, MMICs, wafer-level packages, laminates, antennas and PCBs.

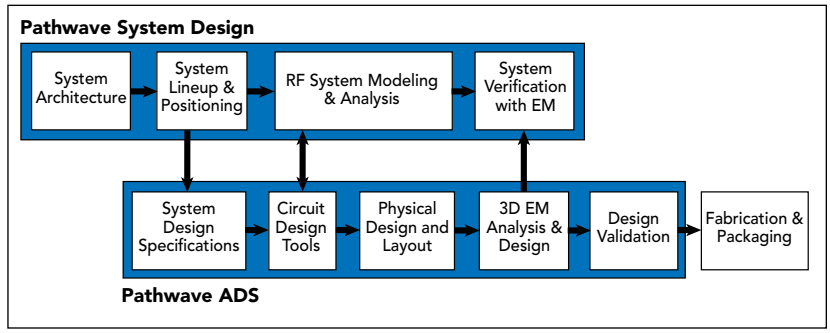
In a typical multi-technology scenario, chips from one technology mount onto different technology modules. Each technology has a substrate with layers, material properties, layout units and database resolution. There must be a mapping between the elements of the different substrates when placing a chip on the top-level module design; then, the layout tool must compute the proper 3D position of objects in the multi-technology design for 3D visualization and EM simulation. A good layout tool can work for both package and IC designs, and an efficient layout environment ultimately facilitates easier assembly of technologies, regardless of the design origin.

One approach EDA software takes is to provide intelligent mounting techniques that adapt when assembling different technologies and integrating databases. Intelligent mounting merges layers at the technology interfaces, such as a MMIC on a package that uses other technology databases. The IC substrate has a ground layer at the bottom, and that is an interface. When the IC mounts onto a package using intelligent mounting, the bottom interface of the IC maps to the top layer of the package, ensuring that the chip has the proper offset. The MMIC must then include design rule checks and layout versus schematic validation at the module level, not just the device, IC and board levels. These processes ensure error-free integration of multi-technology modules for manufacturing sign-off.

EM EFFECTS ON CIRCUIT SIMULATION

In a traditional RFIC design, EM simulators perform simulations for on-chip frequency-sensitive components, such as inductors and capacitors. Complicating the simulation is the modification of the original IC layout to extract and export the components to the EM simulator for analysis. Before the EM analysis can begin, the ports, material properties and simulation parameters must be properly set up. After simulation, multiport S-parameter results must be manually reconnected to simulate the active circuitry. Manual reconnection is error-prone and risks corrupting the design database.

Integration densities and layout infill requirements introduce increased RF coupling effects and longer simulation processes. To reduce simulation time and effort, the leading RF EDA software suites use a technique called EM and circuit "co-simulation." With co-simulation, circuit designers do not need specialists to set up EM tools since correct port types are automatically assigned. Circuit simulations and EM interactions unite in one integrated workflow. Circuit designers can interactively include the 3D EM effects of packaging and interconnects during design exploration, tuning and optimization—not just for final verification of the completed design.



▲ **Fig. 1 Keysight PathWave RF EDA workflow.**

Other new approaches provide circuit designers with the ability to electromagnetically evaluate any portion of their RFIC, MMIC, RF module and RF PCB design without layout modifications using component and net extraction techniques, cutting EM simulation time. Mesh domain optimization can also provide orders-of-magnitude faster simulations of selected (extracted) components and nets.

EM EFFECTS ON SYSTEMS SIMULATION

Most experienced RF designers have endured the challenge of hand modifications to their carefully designed hardware to address cavity resonances and isolation issues. Those modifications can lead to intricate adjustments to multilayer PCBs and mechanics. Early simulation is the way to avoid this rework.

System architects must specify chipset designs to their circuit-level teams to ensure their system specifications are partitioned correctly to the RFIC designers. Modern EDA software suites can verify system performance with circuit-level accuracy by bringing models directly from circuit to system design tools, connecting circuit and system design teams and removing any source of error with a single model format. This workflow step can predict interference and coupling issues through integrated EM analysis, predicting high frequency layout effects on RF system performance. It also gives system designers a powerful troubleshooting tool to pinpoint board and module source coupling before building hardware prototypes.

KEYSIGHT EXAMPLE

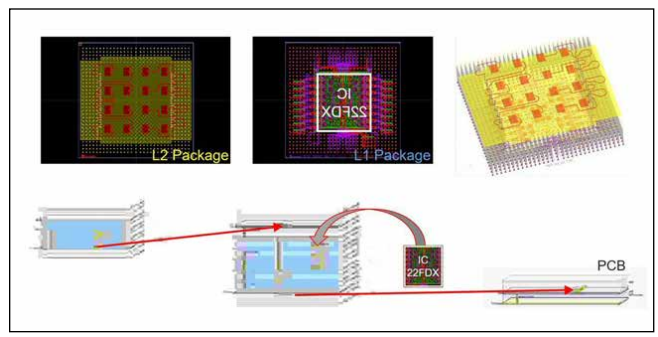
Achieving first-pass success in simulation starts with a comprehensive strategy for circuit and system design. There are many steps in the RF workflow. Minimizing the number of imports and exports during design and simulation can save substantial time and reduce the chance of human input and export errors. ***Figure 1*** illustrates an integrated workflow using Keysight PathWave EDA.

The OpenAccess coalition defines a set of application programming interfaces (APIs) and data formats that facilitate the interoperability of EDA software solutions. Keysight PathWave ADS and PathWave System Design are based on the OpenAccess database architecture and provide efficient assembly and routing of 3D, integrated RF module structures consisting of

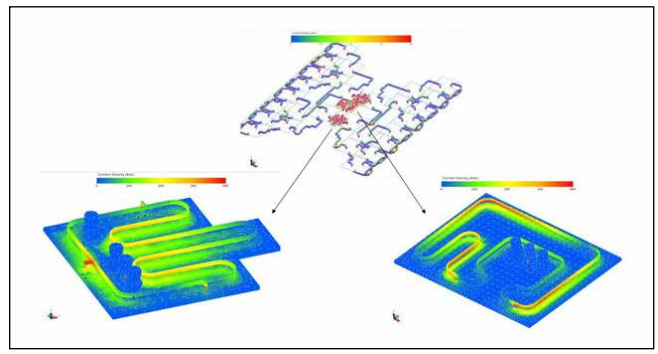
- RFIC and chip-scale antenna layouts based on OpenAccess; for example, Virtuoso and EMPro
- PCB and laminate layouts based on ODB++; for example, Allegro, Expedition and Zuken
- ADS native MMIC and RF layouts.

PathWave ADS enables error-free assembly and 3D avoidance routing to interconnect RFICs, MMICs, laminates, wafer-level packaging, antennas and PCBs into multi-technology RF modules. It is important to be able to assemble multiple adjacent designs, implemented in different technologies, into a single workspace. Keysight's approach to intelligent mounting, called SmartMount, enables drag-and-drop, error-free assembly of mixed-technology components into a "simulate-able" 3D structure by automatically taking care of layer stackup definitions, units and orientation (see ***Figure 2***).

A multifunctional approach to building and assembling packages makes it straightforward for IC designers to account for package effects on IC performance. For example, after assembly, the ADS suite behaves as both a physical IC layout and package design tool, enabling hierarchical substructures as an IC tool and avoidance-route 3D interconnects as a package tool.



▲ **Fig. 2 Intelligent mounting approach with ADS SmartMount. Credits: Design from Global Foundries and Fraunhofer IIS/EAS/IZM.**



▲ **Fig. 3 RFPro in the PathWave Advanced Design System.**

For circuit design, 3D EM circuit co-simulation enables RF circuit designers to electromagnetically analyze any portion of a design interactively without layout cookie-cutting and tedious port setup, ground references and 3D EM simulation parameters. Since the layout does not need modifications for EM simulation, the integrity of the original design is preserved. The introduction of manual modification errors, inherent in other 3D EM simulators, is avoided. ***Figure 3*** illustrates 3D EM circuit co-simulation via RFPro in ADS.

The 3D EM results automatically combine with circuit simulation to analyze the EM effects on circuit performance from packaging, interconnect and coupling. This automation frees the RF circuit designer to do 3D EM analysis and EM circuit co-simulation spontaneously, without manual setup errors. The result is significantly faster EM circuit co-simulation setup—from weeks and months to just seconds and minutes.

A system-level path in the EDA workflow enables advanced virtual prototyping and design for RF system architects, array antenna designers, RF module designers, DSP engineers and system test engineers. The PathWave System Design tool enables RF designers to bring full EM simulated layout effects from their designs or prototypes into the EDA workflow to analyze leakage effects at the system level and pinpoint how to reduce layout risks before committing to hardware.

PathWave RFPro and System Design work collaboratively to perform an EM extraction and map values to the S-parameter file. Once mapped, all nodes versus all nodes can be accurately simulated, including cavity resonance effects caused by the enclosure. With this approach, designers can make precise fixes by visualizing the leakage effects in table form, with node versus node leakage ordered by severity.

SUMMARY

5G and next-generation radar systems use mmWave frequencies with complex modulation and have higher board layer density that push the limits of EM and circuit simulation, system simulation and packaging assemblies. RF system design challenges include multiple antennas, complex modulation, beam steering and sophisticated algorithms.

Keysight's PathWave Design software suite features 3D layout and assembly of multi-technology RF modules, including RFIC, MMIC and PCB. The 3D layout and assembly, together with interactive EM circuit and system analysis, accurately account for EM packaging effects during design. This workflow is an example of how EDA technology is evolving to improve the predictability of the RF design process and reduce design cycles.■

A Dive Into Integrated PA Topologies for 5G mMIMO

Wolfspeed

The race towards hitting 5G speed, capacity, and availability requirements has come with it a number of nascent foundational technologies. At the forefront of these innovations is massive Multiple-Input Multiple-Output (mMIMO), or the outfitting of a base station with hundreds to thousands of antenna elements, each with its own respective transmit/receive signal chain, to maximize spectral efficiency.

The realization of mMIMO requires a high degree of integration with all components in the transceiver, including the power amplifier (PA). This article discusses the various 5G trends and challenges of mMIMO with a dive into the varying integration topologies for the commonly used Doherty Power Amplifier (DPA). Finally, an introduction to Wolfspeed fully integrated PAs is made by showing good RF performance over wide bandwidths.

5G INFRASTRUCTURE TRENDS

Changes in xHaul

In the past, older iterations of 4G base stations (eNodeB) would involve antennas connected to remote radio heads (RRHs) at the top of a cell tower for PHY layer processing that was attached to the baseband unit (BBU) for more complex signal processing. On the network level, multiple RRHs could be served by a pool of BBUs at a far-edge location via the CPRI protocol over a fiber optic link. This centralized RAN topology (C-RAN) has shifted towards a disaggregated network architecture to better fit the varying traffic, throughput, and latency demands of a location. Instead, the 5G architecture involves a function split between the Centralized Unit (CU) and a series of Distributed Units (DU), with the additional potential split of a Radio Unit (RU). In this split, the DU handles low-latency, real-time traffic, while the CU handles non-real-time protocols. This allows for a higher throughput and lower latency communications with a lower layer split (Intra-PHY split). It is known that this split is required in order to support some advanced radio techniques such as Carrier Aggregation (CA) and Coordinated Multipoint (CoMP). For this reason, the enhanced CPRI (eCPRI) protocol was released to better support this functional decomposition.

PA Design Challenges with Advanced Radio Techniques

Power Amplifier (PA) design has been increasingly difficult with modern cellular systems — the OFDM modulation scheme has a high peak-to-average power ratio (PAPR) of around 8-10 dB. This, in turn, requires the amplifier to stay at backoff, well within the linear region to meet adjacent channel power ratio (ACPR) or adjacent channel leakage ratio (ACLR) requirements. The issue with this is when the PA must function within its linear region and away from saturation (its non-linear region), it does not function nearly as efficiently. The use of CA involves the aggregation of available contiguous or non-contiguous blocks of spectrum to increase the throughput and latency of wireless communications in what is typically a populated spectrum (sub-6 GHz). This requires the amplifier to be at additional backoff to avoid the interference of two non-contiguous carriers transmitting simultaneously and to meet strict emissions requirements. Additionally, the amplifier must operate within a wide instantaneous bandwidth, creating a much more complex design challenge to meeting ACLR requirements while maintaining a nominal efficiency.

Linearization/Efficiency Enhancing Techniques

These problems have led to the increased utilization of linearization and efficiency enhancing techniques. The Doherty amplifier configuration is amongst the most popular efficiency enhancing methodology for relatively high PAE deep into the output backoff region. Linearization enhancing methods includes digital predistortion (DPD) where the PA is able to operate near saturation without causing nonlinearities. This is accomplished by distorting the input in such way that the distortions at the output are minimized to increase linearity without compromising PAE.

MMIMO & THE NEED FOR INTEGRATION

Architectural Challenges of MIMO

MIMO has been leveraged for some time now in either a passive antenna topology or an active antenna system (AAS). The issue with passive antenna structures is the increase in channels (e.g., 4T4R, 8T8R, 16T16R, 32T32R), which is directly correlated to a larger antenna count and leads to an increasingly higher port density at the antenna. This, in turn, leads to an array of installation issues as well as unwanted signal degradation from the increasing presence of potential Passive Intermodulation distortion (PIM) sources (e.g., coaxial connector heads). The complexity of this problem only increases with mMIMO. This is where the AAS architecture provides a more optimal solution with an integrated antenna/radio, the only connections that are required to the system are a fiber and DC link for power and control. This differs from older base station architectures where a multi-port passive MIMO antenna structure would be connected to an RRH to finally be routed to the BBU.

mMIMO PA Design Challenges

mMIMO has with it, its own design challenges. Each transceiver chain must be optimized to minimize the inevitable losses, emissions, and non-linearities that will occur. The PAs in this system must then meet linearity requirements while also considering amplifier efficiency, all in a very integrated system package. The typical use of linearity and efficiency enhancing techniques to better meet ACLR requirements without compromising efficiency greatly involves added circuitry which is not typically integrated into the PA package. This is a significant consideration for mMIMO systems as any additional real estate used at the component-level compounds at the system-level with massive number of antennas and respective transmit/receive chains. An integrated PA design with the most commonly leveraged Doherty configuration and DPD linearization technique can be highly beneficial for system engineers in the installation of mMIMO. This can then afford the designer more flexibility in terms of the basic design requirements on power, size, weight, and cost.

Benefits of Using GaN

The use of GaN transistors has already permeated the wireless industry for large, macrocell high powered amplifiers (HPA) and is well positioned to overtake the popularized Si-based LDMOS PA that was previously leveraged. This is due to the intrinsic benefits this substrate has for power applications — the wide bandgap, combined with its high breakdown electric field, power density allow for the handling of large powers all while exhibiting a sufficient electron mobility and saturation velocity to operate at high frequencies. Ultimately this increases the device's reliability, as the amplifier is able to withstand higher junction temperatures for longer periods of time. GaN transistors are capable of this all within a smaller package and at higher frequencies (DC-40 GHz) as manufacturing techniques advance with large wafer diameters and increasingly smaller gate-lengths (e.g., 0.25µm, 0.15µm) fabrication processes. GaN HEMT technology, in particular, has the capability of achieving a higher efficiency at high frequencies, over a wide bandwidth.

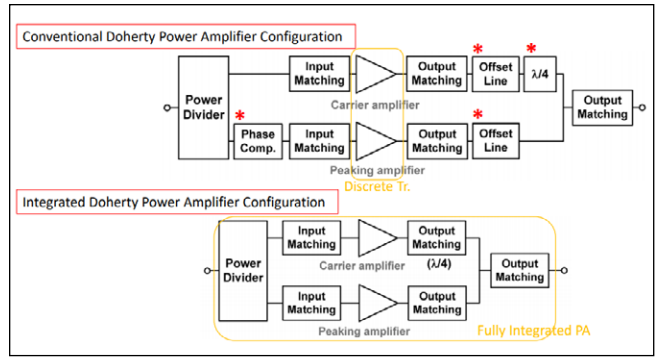


Fig. 1 Discrete (top) versus integrated (bottom) transistor configurations. Maximal bandwidth can be achieved in the integrated example by minimizing the bandwidth limitations of the quarter-wave transformer, phase compensation, and offset lines.

DISCRETE VS INTEGRATED DOHERTY POWER AMPLIFIERS

As mMIMO calls for an increase in integration, smaller form factors are demanded with a high level of linearity and efficiency over a wide bandwidth. Integrating the popularized Doherty PA configuration to enhance efficiency would minimize the 5G New Radio (NR) size and weight and ultimately yield large space savings on the macro-scale in mMIMO installations (See ***Figure 1***). The benefits of small form factor and ease-off-integration come with a number of design considerations though — chief among them, the operating frequency and operating bandwidth of integrated PAs are fixed. Still, this design constraint can be relaxed by minimizing the bandwidth limitation of the quarter-wave transformer, phase compensation, and the offset lines found in the Doherty configuration.

The discrete transistor topology (Figure 1a) has the inherent advantages of increased flexibility as it can be tuned to different operating frequencies. As such, its performance can be better optimized. However, additional input/output matching and combining circuits are required leading to a relatively large form factor, an increase in parts, and an additional layer of complexity towards system integration.

GaN on SiC for Integrated Doherty PA Configurations

It is beneficial to leverage GaN-on-SiC for Doherty PA amplifiers due to its high frequency operation (>3 GHz),

broadband capabilities with a wide instantaneous bandwidth, high power density, and high efficiency. Since SiC has a very high thermal conductivity of 3.7 W/cm-K than that of GaN at 1.3 W/cm-K or Si at 1.6 W/cm-K, these devices can achieve higher power densities more reliably, leading to a relatively larger load impedance than GaN-on-Si devices. This yields to more compact matching circuits, wideband circuit design, and a lower CDS, qualities that ultimately lend itself towards higher terminal impedance and broader band, high frequency operation. Moreover, a higher efficiency can be achieved by employing harmonic impedance tuning — a method that changes the load impedances at the 2nd and 3rd harmonics to optimize the Power Added Efficiency (PAE) of the amplifier.

UNDERSTANDING THE VARYING INTEGRATED TRANSISTOR TOPOLOGIES: AN ANALYSIS

There are several potential compact Doherty combining circuits that can be leveraged to achieve an integrated PA. This includes the following (***Figure 2***):

- Lumped CLC quarter-wave topology[1]
- Quasi-lumped quarter-wave topology[1]
- Lumped LCL quarter-wave topology[1]

Lumped CLC Quarter-Wave Topology

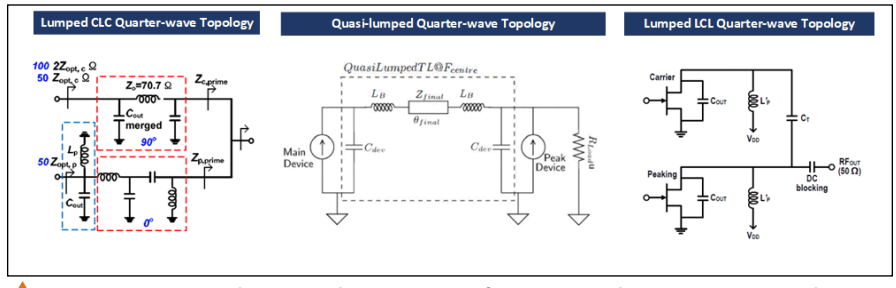
As stated earlier, the bandwidth limiting factors in Doherty PAs are the quarter-wavelength transformer, phase compensation network, and the offset line. The conventional DPA includes the offset line after the quarter-wave transformer in order to compensate for the output capacitance of the transistors and to maintain ideal output load impedance values of both amplifiers. This, however, degrades the effective bandwidth of the system as it has a narrower bandwidth than the quarter-wavelength transformer.

In one iteration of the lumped CLC quarter-wave topology, the output capacitor of the carrier amplifier is merged into the CLC quarter-wave structure while the output capacitor of the peaking amplifier is resonated out with an RF choke inductor. ***Figure 3*** shows the input circuit (3a), output combining circuit (3b), as well as the final schematic representation of the lumped CLC broadband DPA (3c). The use of the quarter-wavelength transformer and the differently biased transistors leads to a need for a phase compensation circuit at the input of a typical DPA. In this topology, the phase compensation network is merged into an input matching circuit.[1]

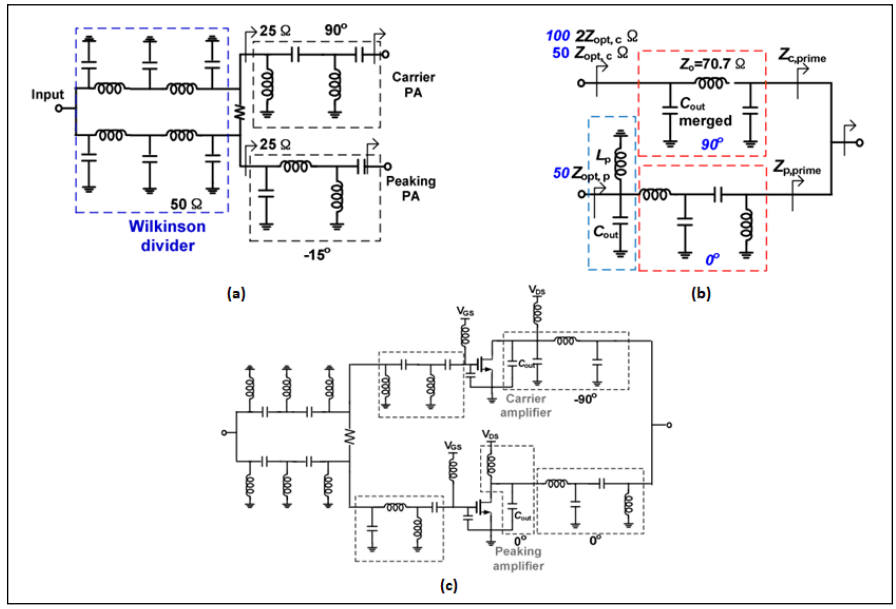
Input Matching Circuit/Phase Compensation Network

The DPA requires a class-C biased peaking amplifier that turns off in low power regions with a class-AB biased carrier amplifier for linearity in the high-power region. However, the gain of the class-C bias grows as the input power increases and because of the turn-on process of the transistor, the input capacitance increases as well, leading to a lower load impedance for the peaking amplifier. Because of this variance in the input impedance with input power level, there is a variance in the division of power between the peaking and carrier amplifiers, ultimately weakening the DPA's broadband performance. Typically, an additional phase compensation circuit is placed at the input of the DPA to eliminate the phase difference caused by the differently-biased transistors and the addition of the quarter-wavelength transformer. Broadband input matching circuits are employed to enable a consistent division of power and input matching across the bandwidth. However, both these additions take up real-estate while the addition of the phase compensation network generally limits the bandwidth of the DPA.

It is desirable for more power to be driven to the carrier amplifier at low powers to prevent the peaking amplifier from turning on early — an event that damages efficiency as the peaking amplifier is drawing more DC current. At high powers, it is also preferable to provide more power to the peaking amplifier in order to ensure proper load modulation and optimal linearity from IMD cancellation. A Wilkinson power divider can accomplish this load modulation by ensuring the input impedance



▲ **Fig. 2 Compact Doherty combining circuits for integrated PA in mMIMO applications.[1-3]**



▲ **Fig. 3 Schematic representation of the input circuit (a), output circuit (b), and entire circuit (c) for an integrated DPA with a lumped CLC quarter-wave topology.[1]**

amplifier is mismatched while the input impedance of the peaking amplifier is matched to port impedance at the maximum output power. This way, maximal power is driven to the peaking path at high powers and the effective bandwidth of the DPA is expanded. This topology includes a two-section high-pass filter (HPF) to both compensate for phase and match the input impedance with the addition of the Wilkinson divider to drive a more dynamic load modulation to maximize efficiency and linearity of the system.[1,5]

Output Matching Circuits

For the output matching circuit, the Z_{Load} impedance is increased to reduce the impedance transformation ratio (ITR). A low ITR has a low Q characteristic, a parameter that is inversely proportional to the BW. By ensuring the Q is the same in the output matching circuit for the carrier, peaking amplifier and quarter-wave transformer, the bandwidth is widened (***Figure 4***). In this topology, the output capacitance of both the carrier and peaking amplifiers are merged into their output matching circuits. However, this slightly altered topology requires the need for an additional offset line in the output path of the peaking amplifier.

Another output matching circuit lumped CLC quarter-wave topology aims to remove the conventionally leveraged offset line in the peaking amplifier in order to meet the size constraints for mMIMO applications. Typically, DPAs will include a quarter-wavelength offset line in the carrier amplifier and half-wavelength offset line in the peaking amplifier after the output matching networks for proper load modulation and wideband performance. This replacement is accomplished by instead using a series inductor (L_{p1}), a shunt inductor (L_{p2}), and a series capacitor (C_{p1}) after the peaking amplifier (***Figure 5***). This way, both the frequency dependent compensation functions that the offset lines provide and the output matching functions can be combined into a more simplified, space-constrained circuit. In this circuit, the impedance at power backoff ($\Gamma_{p,B,O}$) has a similar frequency characteristic to that of a half-wavelength line that acts as an open stub at the center frequency, is inductive at lower frequencies, and capacitive at high frequencies. Moreover, the impedance of the peaking amplifier at saturation ($\Gamma_{p,sat}$) can be transformed into any real impedance lower than the optimal impedance of the peaking amplifier ($R_{opt,p}$).

In implementing this topology, the bonding wires connecting the peaking FET and the circuit are included in the value of L_{p1} while series bonding wires from the carrier FET is included in the output matching network with L_{c1}, L_{c2} while the offset line is formed by the transmission line TL_{c1} (Figure 5b). This leads to a 10mm by 6mm package (after molding) that is implemented on a multilayer epoxy substrate. Final drain efficiencies stand at 53.7% and PAE at 44.8%, both at 8 dB backoff, while the peak output power is 45.3 dBm, and gain is 28 dB (at 8 dB backoff).

LUMPED LCL QUARTER-WAVE TOPOLOGY

Output Network

In a lumped LCL quarter-wave topology (***Figure 6*** (left)), the output capacitance of both amplifiers is resonated out using a shunt inductor. The impedance of the peaking amplifier is inherently high because of this resonance, eliminating the need for an additional offset line. And, instead of using a quarter-wave transmission line, a high-pass LCL circuit is used to perform the same function. This, however, can be simplified by merging the shunt inductors with its adjacent shunt components (Figure 6 (right)). And, because of the large load impedance of the GaN HEMT, the output load impedance can more readily achieve 50Ω.

Input Network: 2nd Harmonic Control Circuit

Several iterations utilizing a lumped LCL quarter-wave topology for the output circuit attempt to mitigate the need for the DPD circuit and maximize linearity by instead cancelling the IM3s of the carrier and peaking amplifiers at the output combining point.[6] A high effi-

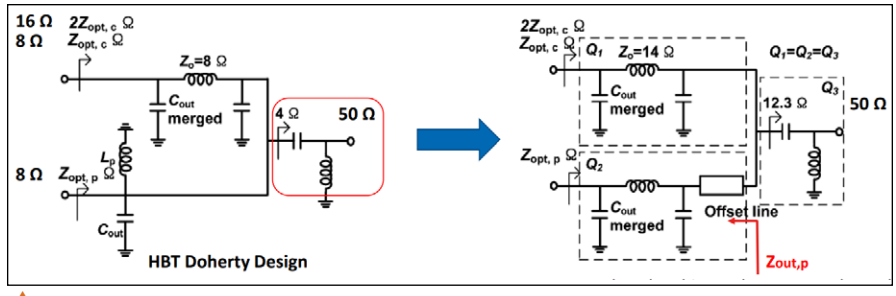


Fig. 4 Different Doherty output networks to delivery 8 ohm at $Z_{opt,c}$ and $Z_{opt,p}$ at a center frequency of 1.85 GHz. The network with an unmated Q (left) requires the use of a quarter-wave transformer with a high ITR, narrowing the bandwidth. The matched Q network (right) expands bandwidth with the addition of an offset line.[5]

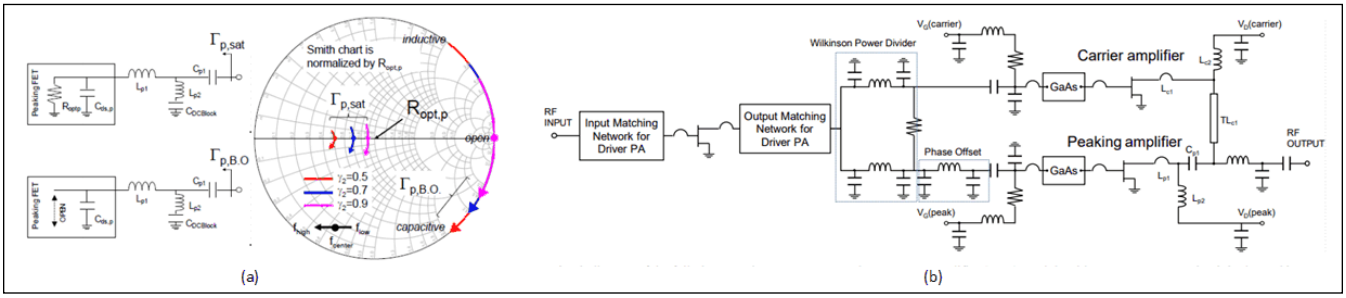


Fig. 5 Simulated results (5a) of the impedance looking into the peaking amplifier from the power combinating node at saturation ($\Gamma_{p,sat}$) and backoff ($\Gamma_{p,B,O}$) at different impedance transformation ratios e8 Full schematic diagram (5b) of alternative DPA.[4]

ciency (up to 70%) can be accomplished by matching the harmonics to the optimum impedances. In some versions, second harmonic input control circuits are realized through a parallel LC network that experiences resonance (open circuit) at the fundamental frequency. This LC network and the bond-wire exhibits capacitive impedance at the second harmonic frequency generates a series resonance for a short-circuit at the second harmonic frequency.[3] Achieving this second harmonic impedance around the short point can improve drain efficiency considerably (***Figure 7***). A tunable capacitor can also be used at the input of the carrier amplifier for multi-band operation. This way, the capacitor can be tuned IM3 performance can be optimized for dual-band capability.[7]

In some lumped LCL topologies, both the input and output include harmonic control circuitry to match the harmonics of the output impedance for the carrier and peaking amplifiers with the optimum impedances for drain efficiency.[7]

QUASI-LUMPED QUARTER-WAVE TOPOLOGY

The quasi-lumped, quarter-wave architecture compensates for the output capacitance of the carrier and peaking amplifiers incorporating it in a transmission line, ultimately forming an impedance inverter. This way, by choosing the right length and characteristic impedance of the artificial transmission line the output capacitances and the bond-ware capacitance can be absorbed. And, rather than be limited by the bandwidth of the conventional half-wavelength transmission line impedance inverter and the bandwidth of the parallel resonator (inductor) that is typically used to eliminate the output capacitances.[2] However, this asymmetrical DPA design can lead to sensitivity issues due to the difference in output capacitances between the carrier and peaking amplifiers.

WOLFSPEED GAN ON SIC INTEGRATED POWER AMPLIFIERS FOR MMIMO

There are some general conclusions that can be gleaned from the previous topologies aiming for an integrated DPA approach. They are as follows:

- The need for a relatively large load impedance
- The need to achieve an adequate load modulation of the carrier amplifier through a 90o phase circuit
- The need to achieve a high output impedance in the peaking amplifier to minimize the power leakage to the FET while ensuring a phase relationship with the carrier amplifier

With all of these considerations there is a general challenge of integrating the phase compensation network, input matching and output harmonic control circuit together on the input side of the DPA. On the output side, combining the output matching network for proper load modulation as well as replacing the offset lines and quarter-wave transformer with discrete inductors and capacitors for comparable wideband performance is the design challenge.

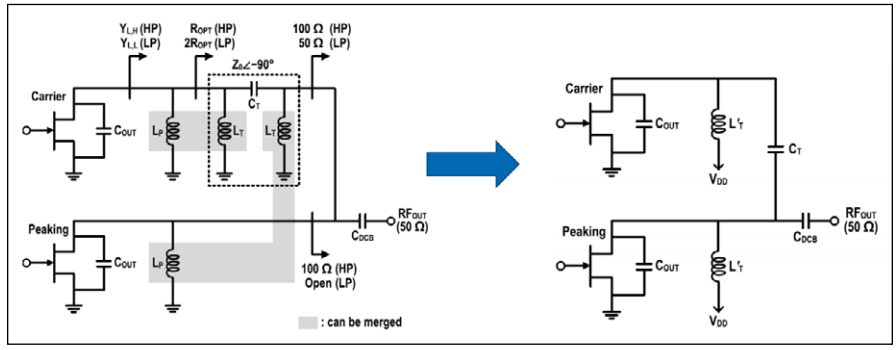


Fig. 6 A π-type low-pass and high-pass circuit (left) is used to replace the quarter-wave transmission line in conventional DPAs, saving on space. This can be further optimized by merging in shunt inductive components (L_p and L_T) into a singular inductor (L'_T) (right).[3]

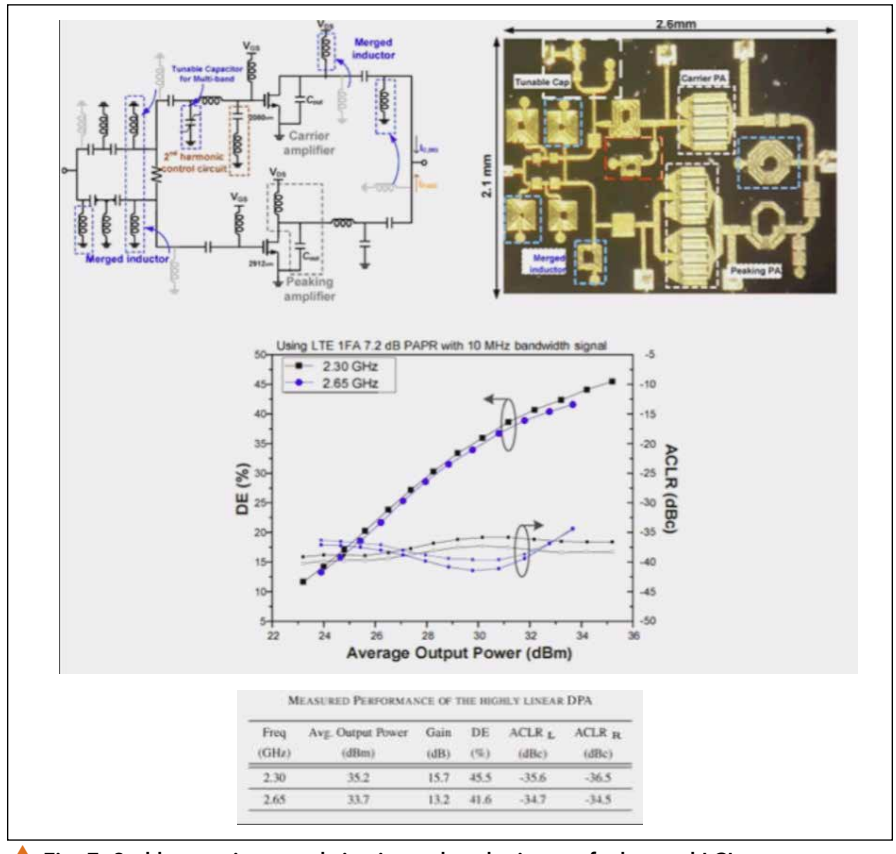


Fig. 7 2nd harmonic control circuit used at the input of a lumped LCL quarter-wave DPA topology. Large drain efficiencies and gain of over 42% and 13.5 dB are achieved respectively at 7.2 dB backoff.[6]

- Wolfspeed integrated DPAs offer two topologies (***Figure 8***):[8]
- A final stage integrated PA (includes only final stage)
- Fully integrated PA (includes both driver and final stages)

Final Stage Integrated PA performance with DPD Linearization

With DPD linearization, a five carrier (5C), 20 MHz LTE signal — 100 MHz instantaneous bandwidth (IBW) — with 8 dB PAPR at a center frequency (f_o) of 3.55 GHz, an ACLR of -55.1 dBc to -56.5 dBc is achieved. This is accomplished as well as an average output power of 39.5 dBm and a high efficiency performance. A ten carrier (10C), 20 MHz LTE signal (200 MHz IBW) at 8 dB PAPR and at a fo of 3.5 GHz, an ACLR of -50.3 dBc to -51.7 dBc is gained (***Figure 9***).

Fully Integrated PA Performance with DPD Linearization

The fully integrated PA tested with a 10C, 20 MHz LTE signal (200 MHz IBW) and a PAPR of 8 dB at a 3.5 GHz center frequency yields an ACLR of -49.9 dBc to -50.3 dBc. An average output power of 37.5 dBm with a high efficiency as well (Figure 10). In other words, it is possible to accomplish an integrated DPA with the input and output driver stages as well as the input and output DPA stages within a small form factor to better fit the needs of 5G mMIMO. Moreover, with the right design and optimization, this can be done under a wide bandwidth signal with up to 300 MHz IBW.

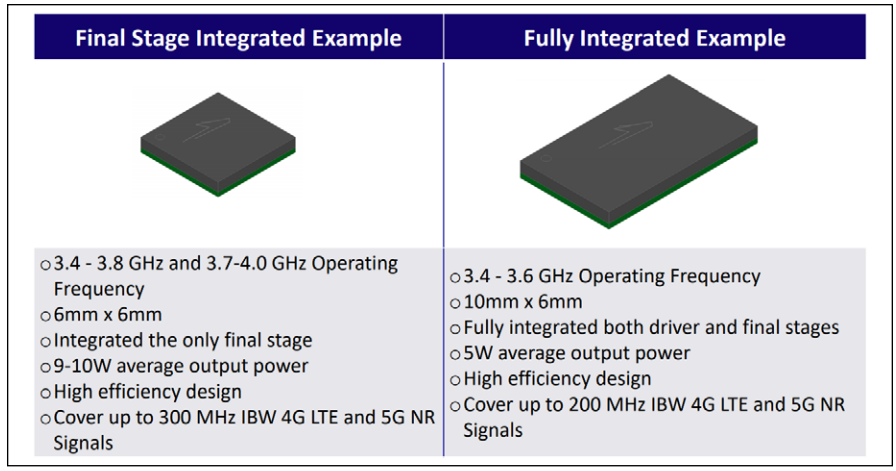


Fig. 8 Final stage integrated PA and fully integrated PA with operation in the S-band and ability to cover 200 MHz and 300MHz IBW 4G LTE and 5 NR signals respectively.

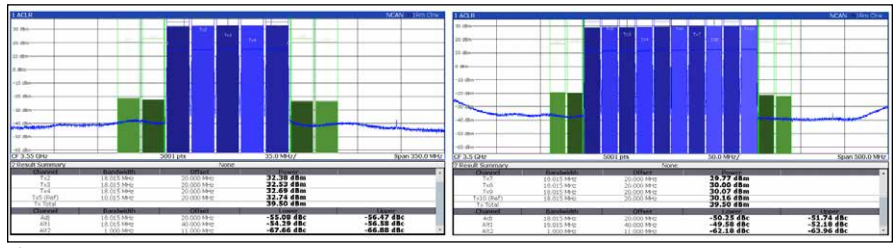


Fig. 9 ACLR plot for Wolfspeed final stage integrated PA with DPD linearization of 5C, 20 MHz LTE signal with 100 MHz IBW (left) and 10C, 20 MHz LTE signal with 200 MHz IBW (right).

Fig. 10 ACLR plot for Wolfspeed fully integrated PA with DPD linearization for 10C x 20 MHz LTE signal (200 MHz IBW).

CONCLUSION

The various 5G infrastructure trends have led to tighter design tolerances with advanced radio techniques, higher performance requirements, tighter restrictions, and more integration. There is a general call for a higher degree of modularity, PAs for mMIMO are no exception to this trend, where PAs are expected to achieve both a high linearity and efficiency all within a small form factor. This leads to the need for an integrated DPA where a number of design challenges crop up when both minimizing and combining the input and output circuits of the carrier and peaking amplifiers while achieving broadband performance. The GaN HEMT using the GaN on SiC is a promising candidate for the integrated DPA with several advantages including a wide bandwidth performance and the ability to achieve higher efficiencies than other technologies. Wolfspeed 5G mMIMO GaN on SiC integrated PAs show high linearity and efficiency under wide bandwidth signals — all within a small form factor.■

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Improving Linearity of a Doherty Power Amplifier with a Dual-Bias Structure

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A novel dual-bias circuit structure increases a power amplifier's video bandwidth while reducing the memory effect, thereby improving its linearity. A Doherty power amplifier (DPA) operating in the 5G communication band (3.4 to 3.6 GHz) and incorporating this circuit achieves a saturated output power of 43 to 44 dBm with a saturated drain efficiency greater than 70 percent. Drain efficiency is 51 to 55 percent at 6 dB power back-off and greater than 43 percent at 8 dB back-off. As output power reaches 42.7 dBm, the adjacent channel leakage ratio (ACLR) is less than -46 dBc combined with digital predistortion (DPD).

For increasing the data transmission rate and the capacity of wireless communication systems, modulation signals with high peak-to-average power ratios (PAPR) are widely applied, and DPAs have become the mainstream for base station power amplifiers.[1-4] Correspondingly, video bandwidth (VBW) and memory effect are two important factors in Doherty RF power amplifier performance.[5]

VBW plays a significant role in the operating bandwidth of the PA and affects the degree of DPD correction.[6] If the instantaneous signal bandwidth is very close to the VBW, PA linearity is seriously deteriorated and is difficult to correct with DPD.[7,8] It can also cause large voltage and current offsets in the active device, resulting in high internal temperatures and component damage.

Several methods to decrease the memory effect and enlarge VBW have been proposed.[9,10] Ladhani et al.[9] obtained wider VBW by directly connecting series resonant circuits to the gate and drain electrodes of a transistor die in a package. This method is based on the design of the transistor current plane and is not suitable for practical circuit design. In addition, an LC resonant bias network has been proposed to diminish baseband impedance for reducing the electrical memory effect;[10] however, the harmful effect of this method is that the fundamental impedance decreases while reducing the baseband impedance. The smaller fundamental impedance causes RF power to leak into the bias circuit. Furthermore, lumped-parameter components with large parasitic elements are difficult to use in RF circuits.

This article describes a high efficiency and high linearity 3.4 to 3.6 GHz DPA with a novel dual-bias network structure to broaden the VBW and minimize memory effects in a wideband DPA when transmitting a 20 MHz A-LTE modulation signal. With the addition of linearization technology, this DPA exhibits good linearity and high efficiency.[11-16]

KEY TECHNOLOGIES

Memory Effect

In a field-effect transistor amplifier, the majority of undesirable memory effects are attributed to the baseband impedance, and the baseband impedance is mainly determined by the impedance of the bias network in the low frequency band.[17,18] When employing

DPD in an RF PA it is particularly important to reduce the memory effect. The baseband impedance, Z, should be short-circuited at low frequencies (see ***Figure 1***); but unfortunately, it is not. The presence of baseband impedance causes the voltage at the drain of the power transistor to change with input signal level. To reduce memory effect, the baseband impedance of the drain bias must be minimized.

VBW

In modern communication systems, wide bandwidth and multi-carrier modulation have been used for high speed data transmission. Nevertheless, the modulation signal bandwidth is limited by RFPA VBW. VBW depends mainly on the equivalent LC resonance of bias networks and transistor internal matching. ***Figure 2*** is the equivalent circuit model of a transistor and a typical bias circuit. The equivalent resonant frequency can be expressed as:

$$f = 1/(2\pi\text{sqrt}(L_m C_{shunt} t)) \quad (1)$$

Where, L_m is the typical bias circuit equivalent inductance and $L_m = L_{shunt} + L_{series} + L_{bias}$. C_{shunt} represents the shunted equivalent transistor package capacitance.

In general, L_{bias} is higher than L_{shunt} and L_{series} by more than two orders of magnitude. So, $L_m \approx L_{bias}$. Therefore, widening of the VBW can be achieved by reducing the equivalent inductance of the bias circuit.

Dual-Bias Network

Optimizing the memory effect requires reducing the baseband impedance, and increasing the VBW requires increasing the equivalent LC resonant frequency. A novel dual-bias network that does this is shown in ***Figure 3***. Compared with a typical bias circuit, the dual-bias network is simply two bias circuits in parallel. From the principle of parallel circuits:

$$Z_{b1} = 2Z_{b2} \quad (2)$$

Where Z_{b1} and Z_{b2} are the drain bias impedances in Figures 2 and 3, respectively. Because the drain node impedance of the dual-bias network is half that of the typical bias circuit, baseband impedance is reduced and the memory effect improved.

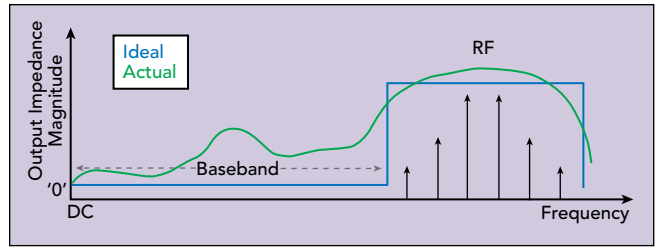
L_{bias} and L_{bias}' in Figure 3 are λ/4 microstrip lines with equivalent parallel inductance of 1/2 L_{bias}. The equivalent resonant frequency is:

$$f = 1/(2\pi\text{sqrt}(L_n C_{shunt} t)) \quad (3)$$

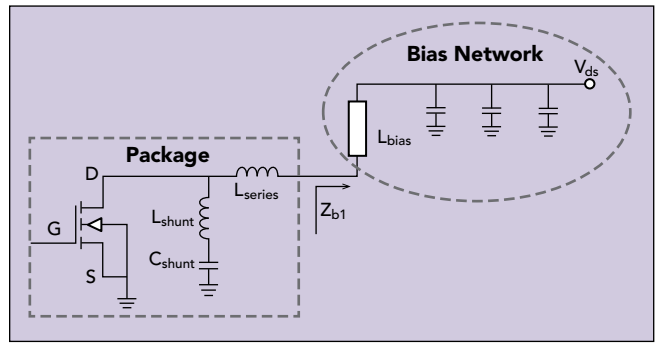
where, L_n is the dual-bias circuit equivalent inductance and $L_n = L_{shunt} + L_{series} + \frac{1}{2} L_{bias}$.

The Cree CGH40010F transistor is used as an example. At a center frequency of 3.5 GHz, the transistor equivalent model is analyzed and the λ/4 microstrip lines equivalent inductance is calculated. L_{shunt} and L_{series} are lower than L_{bias} by an order of magnitude; therefore, L_n can be expressed as:

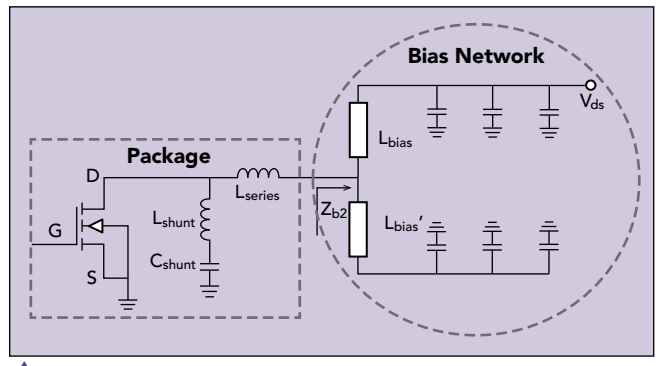
$$L_n = L_{shunt} + L_{series} + \frac{1}{2} L_{bias} \sim \frac{1}{2} L_{bias} \quad (4)$$



▲ **Fig. 1 Ideal vs. actual RF impedance.**

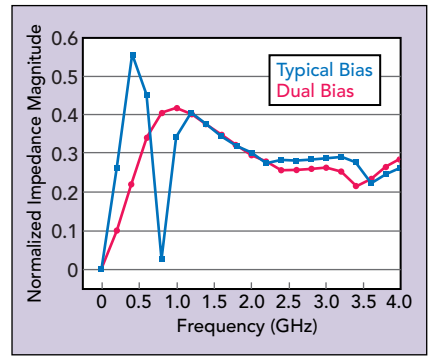


▲ **Fig. 2 Typical transistor bias circuit.**



▲ **Fig. 3 The dual bias circuit increases the equivalent LC resonant frequency.**

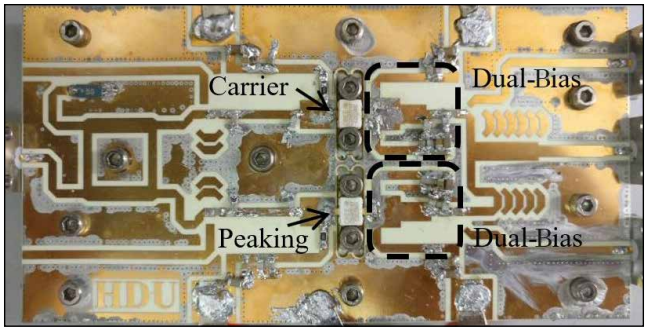
Advanced Design System (ADS) is used to simulate the two bias circuits. The results plotted in ***Figure 4***, show the resonant frequency of the dual-bias network to be about 1 GHz, more than twice the resonant frequency of a typical single bias network, which increases the VBW while reducing the baseband impedance.



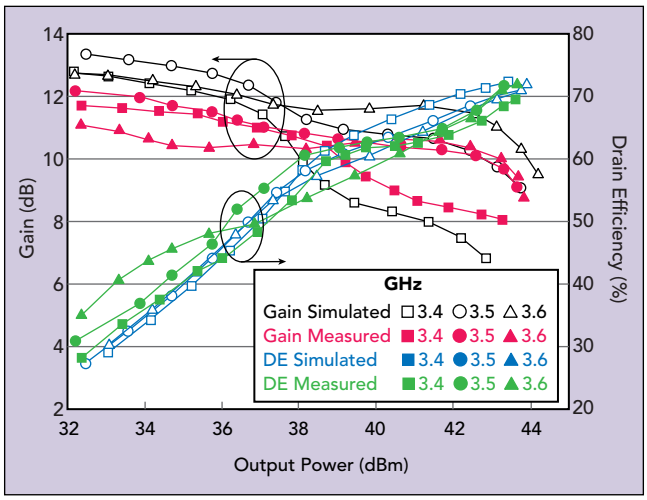
▲ **Fig. 4 Simulated impedance vs. frequency of the typical and dual bias circuits.**

IMPLEMENTATION AND MEASUREMENT RESULTS

The dual-bias network is verified with a DPA designed for 5G mobile communications in the frequency band of 3.4 to 3.6 GHz. ***Figure 5*** is a photograph of the dual-bias DPA. It is fabricated on a 30 mil thick Rogers



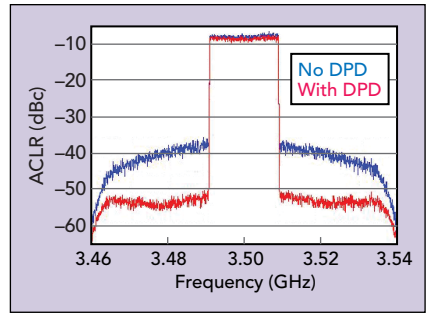
▲ **Fig. 5 Fabricated GaN DPA.**



▲ **Fig. 6 Measured and simulated gain and drain efficiency vs. output power, 3.4 to 3.6 GHz.**

RO4350B substrate with a 3.48 dielectric constant. Cree CGH40010F GaN HEMTs are used for both the carrier and peaking amplifiers. The carrier amplifier is set to Class AB with a gate bias of -2.75 V. The peaking amplifier operates in Class C with gate bias of -6 V. Referring to the transistor datasheet, the drain operating voltages of both amplifiers are set to 28 V.

The curves of the gain and efficiency of the DPA as a function of output power are shown in ***Figure 6***. Saturated output power can reach more than 43 dBm. Compared with the simulated efficiency, at low output power, the measured efficiency is higher and at higher output power, the measured efficiency is about three percentage points lower. The drain efficiency at saturation is above 70 percent. When the output power is backed off 6 dB, it is in the range of 51 to 55 percent. The efficiency is higher than 43 percent when the output power is backed off by 8 dB. Measured gain is slightly lower than simulated. When approaching saturated output power, gain appears to compress, but the average measured gain is greater than 10 dB.



▲ **Fig. 7 Measured ACLR at 3.5 GHz.**

At the 3.5 GHz center frequency a 20 MHz LTE modulation signal with a peak-to-average power ratio of 7.1 dB is used to drive the DPA. The measured ACLR is shown in ***Figure 7***. Upper and lower sidebands are -32.1 and -31.9 dBc, respectively, with an output power of 42.7 dBm. After the addition of DPD they are -46.6 and -47.5 dBc, respectively.

Table 1 provides a performance comparison with other published DPAs, showing improved drain efficiency and ACLR.

CONCLUSION

A new type of dual-bias network structure widens RFPA VBW and reduces the memory effect. To verify this, a DPA operating from 3.4 to 3.6 GHz is designed and fabricated. The ACLR measured with DPD is lower than -46 dBc when using a 20 MHz LTE modulation signal with a PAPR of 7.1 dB. This shows that the dual-bias structure not only widens the VBW and reduces the memory effect, but is also easily implemented.■

ACKNOWLEDGMENTS

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TABLE 1

PERFORMANCE OF PUBLISHED DPAS

Ref.	Frequency (GHz)	Gain (dB)	P_{out} (dBm)	Drain Efficiency (%)	ACLR (dBc)	PAPR (dB)	Modulation Signal Bandwidth (MHz)	Modulation Signal
11	3–3.6	10	43–44	55–66	N/A	N/A	N/A	CW
12	2.6	7–10	51.7	60.4	-35.5	8.3	5	WiMAX
13	2.14	16.6	36.9	57.0	-25	6.5	10	LTE
14	2.2–2.3	11.6–13.6	45	62.9–71	-30	N/A	N/A	N/A
15	2.9	10–15	43.8	64.9	-21	N/A	5	WCDMA
10	0.7–0.86	10–14	49.3	42	-30	7.2	100	LTE
16	3.4–3.6	7–9.5	49.5	60	-29	8.5	100	LTE
This Work	3.4–3.6	8.5–12.2	43.8	> 70	-32	7.1	20	LTE

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Using Off-Chip Passive Components to Maximize GaN Performance & Reduce Cost

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Decades of research and development dedicated to GaN RF power semiconductor technology has led to an increasing supply of affordable RF power devices with impressive performance. GaN semiconductors have reduced material capacitance and enhanced electron mobility, resulting in remarkably low conduction losses, considerably faster switching times and higher frequency-temperature and frequency-voltage characteristics than silicon technologies. Extensive lab testing conducted by numerous sources consistently demonstrates these performance advantages over competing technologies, which has hastened the deployment of GaN power devices in numerous applications. Now, design engineers worldwide are harnessing these compact, low loss and fast switching semiconductors to develop smaller, lighter and more reliable systems that extend the capabilities of solid-state RF power design.

With the many benefits of GaN come a set of challenges with new circuit designs. For example, passive components at the output of a GaN device can reduce the output power of the active component. Even if the passive components don't introduce excessive loss, they can degrade GaN's ability to operate at maximum performance. Some of these design challenges can be overcome by using high performance passive components, such as advanced capacitors and surface-mount technology (SMT) heat pipes. This symbiotic relationship between passive components and GaN RF power devices makes the capacitor selection process critical.

This article addresses several high performance passive component technologies that pair well with GaN to provide impedance matching, bias filtering, DC blocking and thermal control, helping GaN power devices operate optimally.

SINGLE-LAYER CAPACITORS AND IMPEDANCE MATCHING

Single-layer capacitors (SLC) are comprised of a single ceramic dielectric layer with terminations for conductive epoxy attachment and wire bonding. Providing good performance through 40 GHz, they can be used in internal and external configurations—for example, playing an integral role in maximizing the power transfer of a GaN power amplifier as part of the impedance matching networks. When placed inside a device package, SLCs can be elements of a matching network between the lead frame and gate of the transistor, helping provide a broadband impedance match at the input of the device. Used outside the package, SLCs can be used for impedance matching, DC blocking and broadband bypassing.

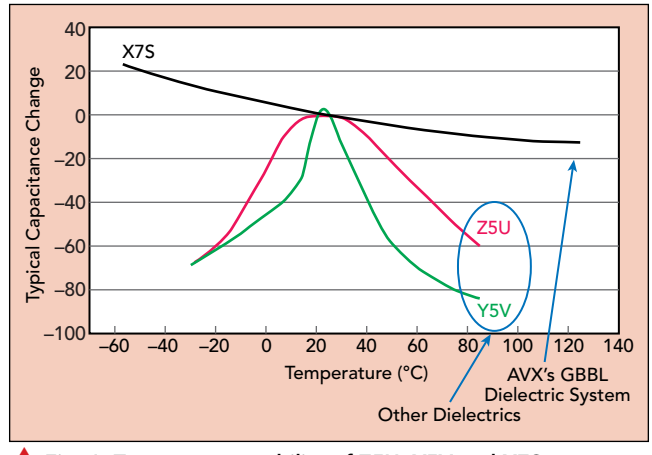

Fig. 1 Temperature stability of Z5U, Y5V and X7S dielectrics. The GBBL material system has X7S temperature characteristics.

SLCs can be configured as single, dual or multiple SLC arrays to minimize component count.

Most of the electrical characteristics of SLCs are determined by the ceramic dielectric used for their construction. The two most common dielectrics are SiO_2 and C0G (NP0) EIA Class I temperature-compensating ceramic. Both have high temperature stability (0 ±30 ppm/°C), ideal for impedance matching where temperatures are high and thermal stability is critical. A new type of dielectric, the grain boundary barrier layer (GBBL) material system, has demonstrated noteworthy performance as a replacement for the general-purpose Z5U and Y5V ceramic dielectrics where bulk capacitance is a concern. A typical GBBL dielectric exhibits X7S temperature characteristics with better temperature stability compared to the Z5U and Y5V dielectrics (see ***Figure 1***).

SLC terminations are typically comprised of sputtered TiW/Au or TiW/Ni/Au. This combination of sputtered materials yields thin, high-quality termination surfaces with excellent adhesion, essential for conductive epoxy attachment and wire bonding, particularly with high-power RF devices subject to severe temperature cycling. The terminations can be bordered, which means the metallization does not extend to the capacitor edges, or non-bordered, which means it does (see ***Figure 2***). Bordered SLCs minimize the chance of conductive epoxy climbing the sidewalls to touch the top plate and short the capacitor. Ideally, epoxy fillets should flow about halfway up the side of an SLC, but since MIL-SPEC requirements don't specifically specify conductive epoxy fillet height on die edges, using bordered SLCs can avoid the possible negative outcome from overflow.[1] Non-bordered SLCs are typically used in source bypass configurations because they reduce the bond length between the top termination and the active device.

BULK CAPACITORS FOR BIAS FILTERING

GaN power devices require a stable bias voltage for optimum operation. Since bulk capacitor banks are

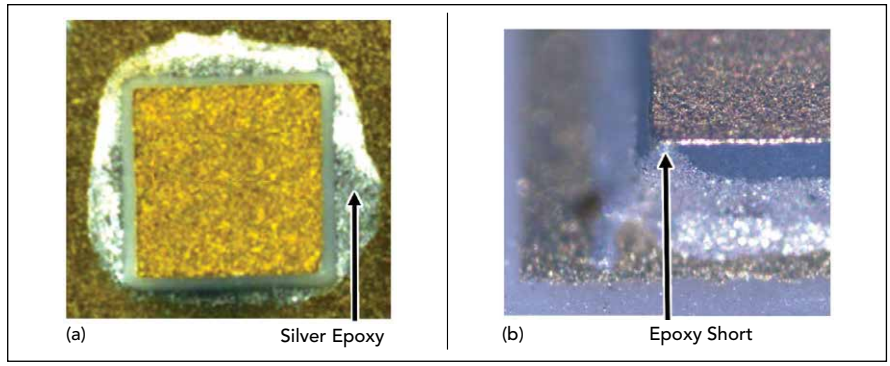

Fig. 2 Bordered (a) and non-bordered (b) SLCs. Excess conductive epoxy can climb up the sidewall of a non-bordered SLC and cause a short. *Source:* TJ Green Associates, LLC.[1]

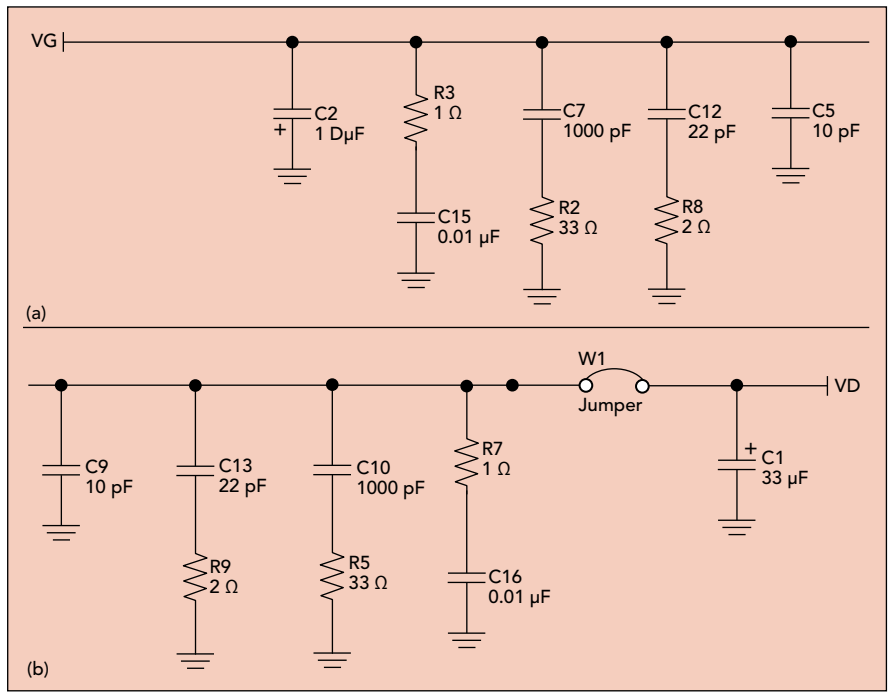

Fig. 3 Gate (a) and drain (b) bias filter banks. *Source:* Qorvo.[2]

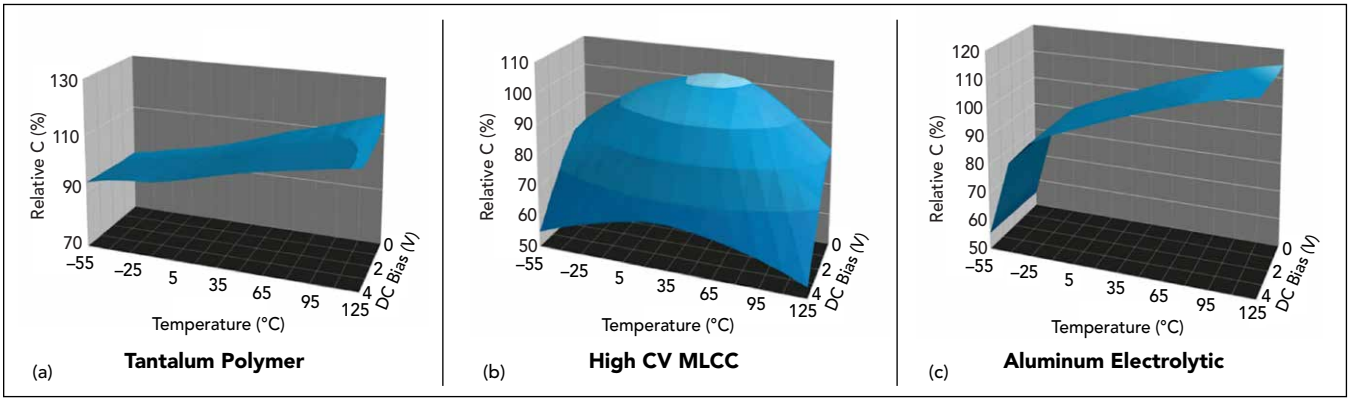

Fig. 4 Capacitance stability, DC bias and temperature performance for tantalum polymer (a), high-CV MLCC (b) and aluminum electrolytic (c) capacitors.

stable with voltage and temperature and have good aging characteristics, they are often used to filter bias line noise and provide a fast source of charge to supply the high current changes ($\Delta i/\Delta t$) in a power amplifier (see ***Figure 3***). The transient response of these filter capacitor banks is determined by the combination of high capacitance and high frequency response. Bulk capacitors suitable for voltage bias banks include high-CV multilayered ceramic capacitors (MLCC) and tantalum, tantalum-polymer, aluminum and aluminum-polymer electrolytic capacitors (see ***Figure 4***).

While high-CV MLCCs can achieve the capacitance ranges required for many bias networks, they don't provide stable capacitance values across operating conditions such as temperature, time and DC bias.[3] For example, the capacitance stability of a 100 µF X5R MLCC can vary from 100 µF at 25°C to approximately 85 µF at -55°C and 80 µF at 125°C. High-CV MLCCs also suffer from DC bias voltage effects that can significantly reduce the capacitance value present in the circuit. For example, the capacitance value of a Class II MLCC can decrease by 35 to 65 percent at the fully rated DC current. Additionally, low voltage AC ripple current can further reduce the capacitance of high-CV MLCCs by another 5 percent, and aging can reduce the capacitance by another 2 to 5 percent per decade. Depending on the operating conditions and the MLCC chosen, all these losses combined with the temperature coefficient can reduce the total expected capacitance of high-CV MLCCs by approximately 80 percent.

The remaining bulk capacitor options suitable for bias filtering include traditional and polymer versions of tantalum and aluminum electrolytic capacitors. Although this article focuses on tantalum bulk capacitors for bias filtering, aluminum capacitor technology and performance are also improving. Tantalum capacitors have size, weight and stability advantages over traditional aluminum electrolytic capacitors. For example, tantalum capacitors have an average capacitance of 0.6 µF/mm^3 compared to miniature aluminum electrolytic capacitors, which have an average capacitance of 0.1 µF/mm^3. Tantalum-polymer capacitors exhibit approximately one-eighth the equivalent series resistance of traditional tantalum capacitors, meaning a current capacity approximately 8× of traditional tantalum capacitors. Advances in tantalum-polymer capacitor technologies have also extended the voltage rating of miniature SMT capacitors to 125 V. While traditional tantalum capacitors require 50 percent derating, tantalum-polymer capacitors rated up to 16 V only require 10 percent derating for polymer substrate devices and 20 percent derating for those rated for greater than 16 V operation.

Tantalum and tantalum-polymer capacitors are available in multiple case sizes with reduced height profiles relative to aluminum electrolytic capacitors and with novel lead frame packages that have dramatically lower inductances than aluminum electrolytic capacitors (see ***Table 1*** and ***Figure 5***). This enables bulk capacitor designs with better fit. As such, both tantalum and tantalum-polymer capacitors are highly competitive with aluminum electrolytics and well suited for use in GaN power amplifier designs, despite their derating.

UNIQUE CAPACITORS AND DC BLOCKING

Another passive component requirement for GaN power amplifiers is DC blocking. DC blocking in circuits operating at higher frequencies and wide bandwidths requires stable, low loss capacitors that can be easily configured to the circuit. Three unique capacitor technologies are worth considering: ultra-broadband capacitors (UBC), metal-insulator-metal (MIM) capacitors and metal oxide semiconductor (MOS) capacitors (see ***Figure 6***). While there are additional options, these three types have proven to be practical for DC blocking.

UBCs — UBCs have a multilayered ceramic dielectric form factor that is compatible with standard printed circuit board manufacturing, including fully automated, high speed pick-and-place processing. They are available in 0201 and 0402 package sizes to match transmission lines, respectively, rated for 10 and 100 nF and they have ultra-low insertion loss, flat frequency response and excellent return loss from 16 kHz to approximately 70 GHz (see ***Figure 7***). UBCs are an optimal passive component for DC blocking, DC coupling, bypass and feedback circuits in GaN power amplifiers.

MIM Capacitors — MIM capacitors are small, have low loss and can be used to compensate for the inductance effects of wire bond attachments, making them useful for DC blocking in high frequency transmit and receive stages. MIM capacitors use quartz, alumina or glass substrates to minimize loss and have a transmission line wire bond pad with backside ground to extend

TABLE 1

TANTALUM CAPACITOR CASE SIZES AND INDUCTANCE

Case Size	Inductance (nH)
Standard Devices	
A	1.8
B	1.8
C	2.2
D	2.4
E	2.5
F	2.2
G	1.8
H	1.8
K	1.8
N	1.4
P	1.4
R	1.4
S	1.8
T	1.8
U	2.4
V	2.4
W	2.2
X	2.4
Y	2.4
5	2.4
Low-Profile Devices	
K	1
L	1
M	1.3
N	1.3
O	1
S	1
T	1
Multianode Devices	
D	1
E	2.5
U	2.4
V	2.4
Y	1
D	1

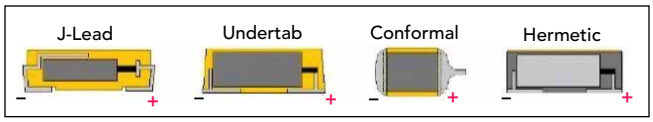

Fig. 5 Tantalum capacitor packaging options.

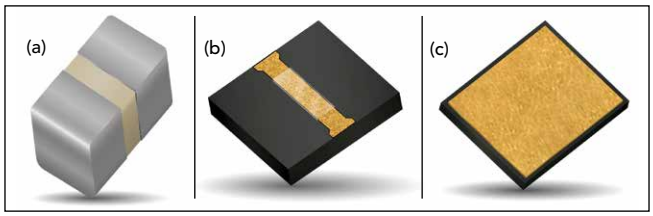

Fig. 6 UBC (a), MIM (b) and MOS (c) capacitors.

the frequency performance and reduce loss. Copper traces maximize conductivity, and front and backside gold metallization are compatible with high integrity epoxy, gold wire or ribbon attachment. They have 60 ppm/°C temperature stability with capacitance values from 0.3 to 15 pF and up to 100 V operating voltage. Custom capacitors can be designed, using a 50 to 100 pF/mm^2 capacitance to area ratio.

MOS Capacitors — MOS capacitors are SLCs with SiO_2 dielectrics and are small, temperature-stable capacitors with high Q, high breakdown voltage and low leakage. Manufactured with copper terminations in standard or custom patterns, MOS capacitors can be as thin as 127 µm for integration in 2.5D and 3D multi-chip modules, enabling higher frequency and lower power designs—potentially eliminating the wire bonds to the capacitor to reduce series inductance and extend the frequency response. Other termination options are gold or aluminum metallization on the top side and no metallization silicon, gold on bare silicon or chrome-gold on the bottom. Standard MOS capacitors are compatible with epoxy and solder die attachment and gold or aluminum wire bonding. Standard sizes and capacitance values range from 0.010 to 0.070 in.^{2} and 1.0 to 1,000 pF, respectively.

SMT HEAT PIPES

A signature benefit of GaN power devices is their ability to deliver high power in a small package. This can generate a massive amount of heat in a small area, requiring thermal control methods to remove, spread and couple the heat from the active device to get maximum performance and ensure reliability.

The thermal challenges of GaN can benefit from novel solutions like miniature SMT heat pipes.[4] Miniature SMT heat pipes are a cost-effective solution for providing additional heat flow from the pins of an active device. Unlike traditional heat pipes, SMT heat pipes deliver high thermal conductivity with reduced parasitic capacitance, higher insulation resistance and high breakdown voltage. The small size of the SMT heat pipe supports the requirements for small size, weight and power (SWaP) designs. Although performance depends on the case size, the typical parasitic capacitance for the standard 0402, 0603 and 0805 EIA sizes is just 0.04 to 0.13 pF and the typical thermal conductivity is from 40 to greater than 500 mW/°C.

Miniature SMT heat pipes are available with several terminations: Sn/Ni/Pt, Ag/Pt and non-magnetic Ag. Custom SMT heat pipes have been designed to optimize the heat flow around MMICs, other high-power devices have been developed in case sizes spanning 0302 to 3737.

To illustrate the effectiveness of the SMT heat pipe, AVX engineers performed infrared (IR) measurements on an ultraminiature, high performance GaN power amplifier MMIC rated for 100 W output power. The MMIC was operated with a CW signal for 20 seconds at the amplifier's center frequency, measuring the thermal rise with no heat pipes and using three Q-Bridge SMT heat pipes. Using the heat pipes, the IR measurement showed a 38°C decrease in MMIC temperature without any design modifications (see ***Figure 8***), from approximately 80°C with no heat pipes to 42°C using the heat pipes. Neither the MMIC nor the larger power amplifier assembly were designed to include the Q-Bridge SMT heat pipes, i.e., the test was run with an existing design. Arguably, greater heat reduction could have been demonstrated if the power amplifier had been designed to include these SMT heat pipes.

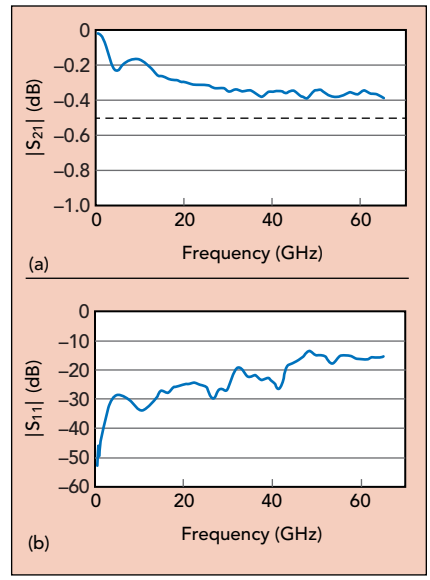

Fig. 7 Typical $|S_{21}|$ (a) and $|S_{11}|$ (b) of the 550L series UBCs.

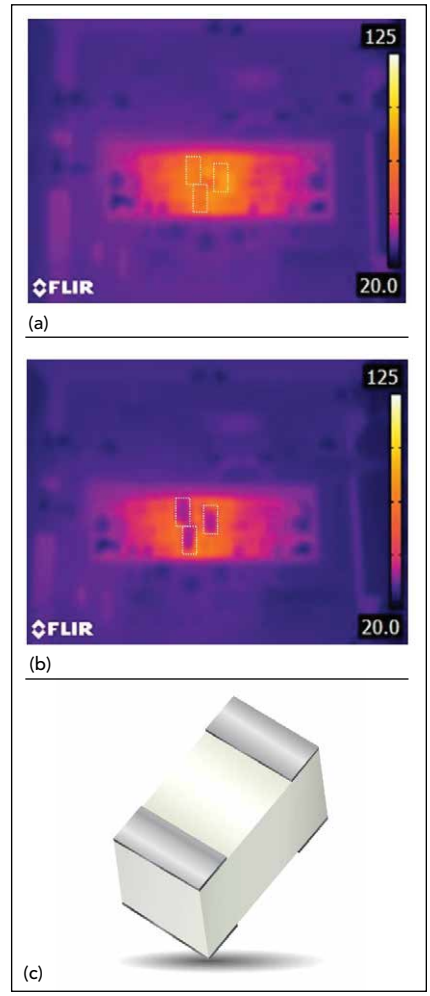

Fig. 8 IR thermal scan of a 100-W GaN PA MMIC without heat pipes (a) compared to the PA using three heat pipes (b). Q-Bridge SMT heat pipe (c).

SUMMARY

GaN RF power devices have been proven through extensive lab tests and products, hastening their deployment for defense and commercial applications, in turn driving prices down and increasing accessibility. To fully realize GaN's impressive performance—reduced capacitance, higher electron mobility, low conduction losses, faster switching and higher frequency-temperature and frequency-voltage characteristics than silicon—engineers must pair GaN devices with high performance passive components. Passive components are important circuit elements for impedance matching, bias filtering, DC blocking and thermal management. Without paying attention to the effects of these passive components, designers risk limiting the technology from reaching the full capabilities of its performance.

The development of new material systems, such as the GBBL ceramic dielectrics for SLCs and conductive polymers for tantalum bulk capacitors, are enabling designers to mitigate these potential performance limitations. New capacitor sizes and package styles are enabling smaller layouts to support SWaP requirements and improve electrical performance. New devices like SMT heat pipes are expanding the solutions available for removing, spreading and coupling the heat from the higher power density of GaN—improving both performance and reliability.

As GaN device technology continues to evolve and deliver improved performance, new and improved passive component technologies will be engineered to support these impressively compact, low loss and fast switching semiconductors, leading to the next generation of smaller, lighter and more reliable RF power amplifiers.■

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First-Pass RF GaN Design Needs Accurate Models

Wolfspeed

GaN HEMTs have been outcompeting and replacing LDMOS, GaAs, and SiC devices in RF power amplifier designs with their much-sought-after characteristics, including high-voltage operation, high breakdown voltage, high power densities of up to 8 W/mm, transition frequencies (fT) of up to 55 GHz, and low quiescent current.

To capitalize on these advantages, however, engineers must be able to design keeping in mind GaN devices' self-heating tendency as well as cater to the impact of nonlinear dependence of device parameters on signal level, thermal effects, and ambient conditions. When modelling and simulating the power amplifier, predictability of large-signal performance can significantly shorten effort and time spent tuning the design with physical measurements on the bench.

When accurate device models are available, designers can cut down device characterization time, linking layout optimization to the desired performance. They can accurately conduct load-pull simulations, create matching networks, and generate EM simulation. This enables modelled results to closely match measured results and helps designers achieve first-pass design success.

TYPICAL FLOW FOR FIRST-PASS DESIGN

Design for first-pass success starts with setting up the device model for simulation in software, like Cadence's AWR Microwave Office or Keysight's Advanced Design System (ADS). This is done by specifying the back-of-the-case temperature at the hottest point (T_{case}), the thermal resistance stated on the datasheet for the operating conditions (R_{th}), and the operating voltage (V_{dn}). The designer must understand the various device ports to set it up for simulation.

When using devices in SMT packages, simulation accuracy can be increased by setting up the device with the EM ground pad that would be used on the PCB for mounting the device. Modeling the source inductance is important because it affects the device's stability as well as its high-frequency performance.

After this, a load-pull and biasing analysis is conducted followed by matching circuit design and measuring performance. Once thermal and EM analyses are complete modeled results are compared with measurements to ensure design goals are met.

The design process described below is based on the demonstration of a 30 W power amplifier design using Wolfspeed's CGHV27030S GaN HEMT for a Mode S 1030/1090 avionics application. The transistor is a 50 V surface-mount device in a DFN package. The software used is AWR Microwave Office.[1]

LOAD PULL & BIASING

The load-pull template in AWR allows designers to derive the locus of different impedance points. Device performance can be monitored against changes in source and load impedances to select the optimum values.

The load-pull template is set up by:

1. Picking an input power that is reasonable for the design. For the 30 W amplifier design example that delivers 18 dB of power gain, 27 dBm of input power was chosen.
2. Setting impedances to zero, as ideal impedances are unknown.
3. Setting the output/load impedance (Z) to the value the amplifier must be matched to, typically 50 Ω.
4. Selecting one frequency at a time for each simulation, starting with the middle of the band.

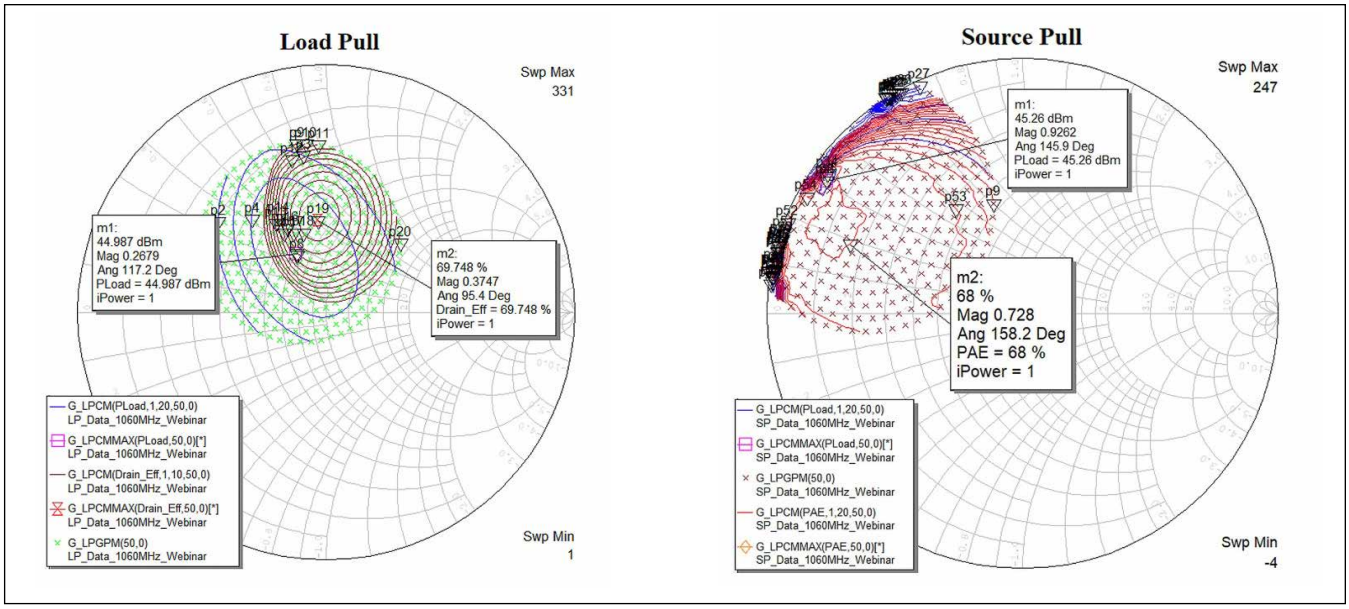

Fig. 1 Load- and source-pull charts allow designers to pick impedances that best match their design goals.

5. Selecting the operating voltage, the gate voltage to be adjusted to desired bias conditions, and the quiescent drain current (Idq).
6. Choosing an RC network that achieves the desired balance between gain and stability.

Load pull and source pull are run multiple times until they converge on an ideal impedance that satisfies the design goals for efficiency and power (***Figure 1***).

The resulting Smith charts from the load- and source-pull simulations represent the achievable efficiency and power for those impedances. From this, a load and source impedance that achieves designs goals can be chosen. Using the load-pull impedances, designers also examine how different bias conditions affect performance.

For instance, an engineer may select a source impedance that offers optimal efficiency. Alternatively, the designer can select a different load impedance that offers an equal trade-off between peak power and peak efficiency. A gate bias that offers a balance between power gain and drain efficiency, as well as good gain flatness over power, is usually a good choice.

MATCHING CIRCUIT

The next step is to create a matching network that transforms, typically, 50 Ω to the complex conjugate of the source impedance. Designers may start with a real microstrip network or reach it by converting from an ideal LC network or an ideal microstrip network. The real microstrip provides parasitic qualities that are seen when testing in the lab. Switching from an ideal to real microstrip network could affect performance, and redesigning the microstrips may be required. At this point, designers also switch from ideal RLC components to the real ones.

Because SMA connector and GaN device gate pads have fixed sizes, layout must be done around those constraints. The microstrip lengths and widths are chosen to minimize the use of components while providing a match from the SMA to the gate pad.

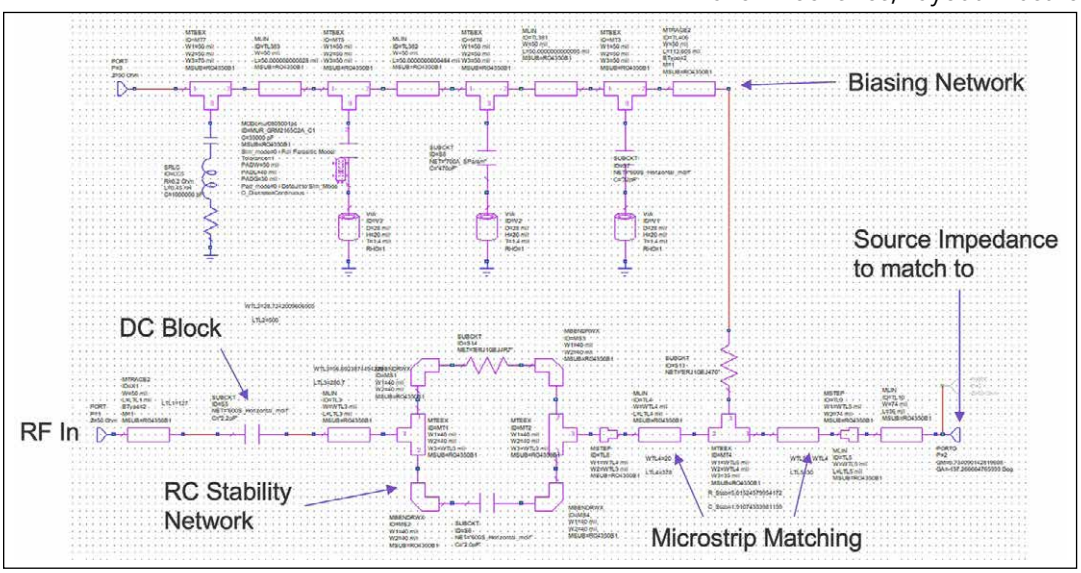

Fig. 2 A typical input match circuit showing the biasing network, RC stability network, microstrip matching, and the source impedance in the AWR Microwave Office environment.

In the example input match shown in ***Figure 2***, the top right is a biasing network comprising a microstrip line, decoupling capacitors, and a gate resistor. The RF In is tied to a microstrip line, followed by the DC blocking capacitor to prevent any DC leak-

ing back into the RF, the RC stability network, the microstrip matching, and, finally, the source impedance.

Similarly, on the output side, the SMA and drain pad sizes are fixed and need to be designed around. The microstrips are chosen to create the match between the two pads using a minimum number of components. The output matching circuit also comprises a biasing network, DC blocking capacitors before an RF Out, microstrip matching, and, finally, the load impedance to match.

Simulations are run for output power, efficiency, and gain, as shown in ***Figure 3***, and for small-signal gain and return loss over the targeted frequency band. For the PA design demonstration, a CW profile was chosen because it provides a more stressed performance than the Mode-S signal.

The simulation is done at both 25˚C and 85˚C. At the higher temperature, performance is expected to decrease across the three measures of output power, efficiency, and gain and therefore must be reliably predicted.

THERMAL ANALYSIS

If the GaN HEMT is not thermally viable in the design, other performance parameters will not matter. Vendors like Wolfspeed provide a junction thermal resistance value ($R_{\theta jc}$) for their transistors. Designers use it to calculate junction temperature[2] as:

$$T_j = T_c + (P_{diss} \times R_{\theta jc})$$

Where Tc is the case temperature and Pdiss is the dissipated power calculated from measurements by subtracting output power from input RF power and DC power.

It is essential that T_j meets the die's safe operating conditions, which would allow a mean time to failure of more than 1 million hours. Wolfspeed, for instance, specifies a maximum T_j of 225°C for its GaN HEMTs and calculates $R_{\theta jc}$ value by correlating and validating FEA simulation analyses with measurements from an IR camera.

EM ANALYSIS

The final step before committing the design to hardware is EM analysis. If using AWR Microwave Office, it's Axiem EM analysis provides a detailed simulation that accurately captures parasitics, coupling, and other effects from driving RF through the design. It is preferable to run EM simulation on the entire design, including the simulation of the eventual PCB layout.

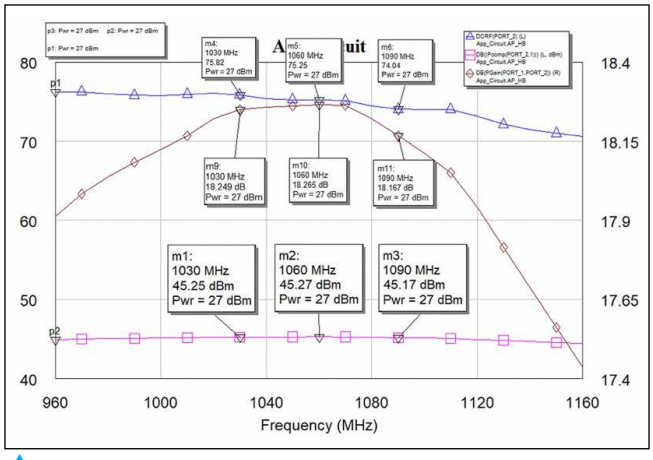

Fig. 3 A example of simulated performance: output power, efficiency, and gain (25°C). In this case, simulation was done at Pin = 27 dBm, Vdd = 50 V, Idq = 128 mA.

AWR's EM extraction tool takes the microstrip design and generates an EM layout. Although the actual board layout might differ from the microstrip design, this method includes EM simulation of the matching network that has the biggest impact on performance.

The tool also allows importing of DXF files from AutoCAD. This method includes parts of the circuit that have minimal impact on performance, lengthening simulation time. But it ensures that the EM structure matches the PCB.

Key points to remember are:

- Setting the frequency of the EM to run from DC to the third harmonic of the design.
- Simulating the mesh to gain insight into the EM simulation before running the full EM. This also reveals errors in layout or EM simulation, such as port errors.

The aim of this design flow is to achieve a simulation that is a close match to the eventual physical measurements for both large-signal characteristics of power output, gain, and efficiency against frequency as well as small-signal characteristics of S-parameters against frequency.

DEVICE MODELS AFFECT SIMULATION ACCURACY

Although device performance in specific applications is determined traditionally by developing test hardware and conducting physical load-pull measurements, it is a cost-, time-, and effort-intensive exercise. A large-signal device model that closely matches real measured performance can reduce development costs, allow in-depth what-if analysis to validate device choice, and reduce design cycles. But the accuracy of device models dictates the availability of these benefits from simulation.

The device model must be accurate in modelling both small-signal and large-signal behavior and must have the following characteristics:[3]

1. Large-signal load pull and power drive-up must have been verified at various frequencies and device sizes to ensure accurate large-signal scaling.
2. To be successful in scaling by a large ratio, the unit cell model must be very closely correlated with measured data in a wide range of operations relevant to the application.
3. The non-linear model must fit small-signal parameters over a range of bias voltages in which measurements are performed using CW conditions.
4. In addition to the three FET ports (gate, source, and drain), the models should provide access to intrinsic drain-current and drain-voltage waveforms, as well as the junction temperature of the die.
5. The model must include built-in process sensitivity and non-linearity on individual elements as needed.
6. An accurate, physically derived package model, including package parasitic interconnects comprising different tools like S-parameters, is critical.

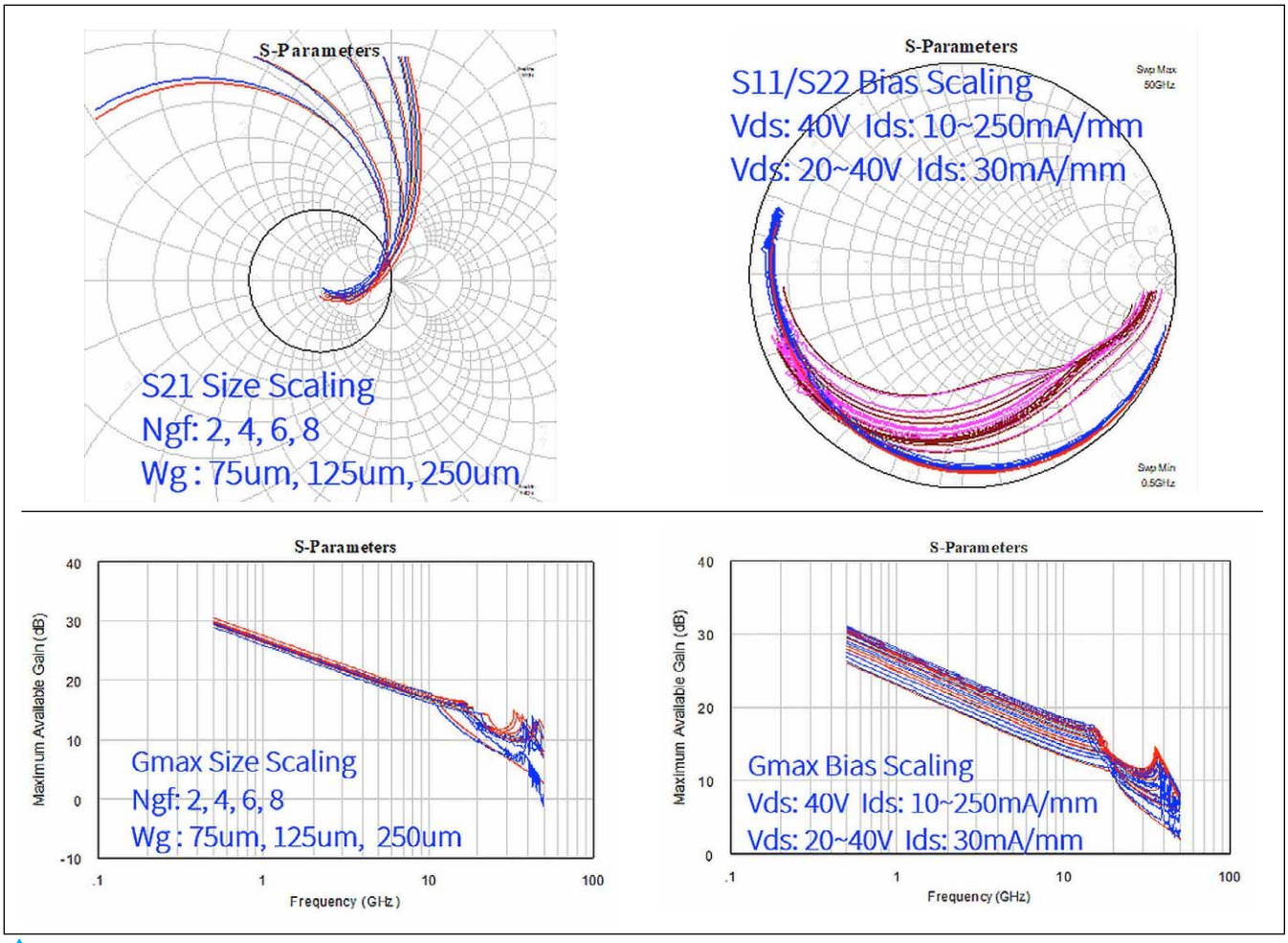

Fig. 4 An example of the desired small-signal (top) and large-signal (bottom) plots showing modeled (red) and physical (blue) device performance characteristics

An example of a closely matching model to measured performance is shown in ***Figure 4***. The Smith chart on the left shows how closely the modelled data should follow the measured data in both magnitude and phase across different gate widths and bias values.

TOOLS EASE THE LEARNING CURVE

Vendors often invest in tools and resources to help engineers design with their products. The first-pass design flow discussed here is described in much greater detail in the webinar "Power Amplifier Design Flow Using GaN Large Signal Models in AWR." Further resources and tools are available on this RF Devices Tools & Support page.■

References

1. Wolfspeed, "Power Amplifier Design Flow Using GaN Large Signal Models in AWR." Source: https://www.wolfspeed.com/knowledge-center/article/power-amplifier-design-flow-using-gan-large-signal-models-in-awr
2. Wolfspeed, "Thermal Considerations for High-Power GaN RF Amplifiers." Source: https://www.wolfspeed.com/knowledge-center/article/thermal-considerations-for-high-power-gan-rf-amplifiers
3. Wolfspeed, "GaN HEMT Large Signal Models." Source: https://www.wolfspeed.com/knowledge-center/article/gan-hemt-large-signal-models

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