FABLESS CHALLENGES OF INTEGRATING COMPLEX SILICON INTO THE IC PACKAGE, EVEN THE SYSTEM PCB

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THE NEED FOR INTEGRATION AND OPTIMIZATION

As the world continues to demand more performance, bandwidth, and capacity from smaller, lighter, and lower-power products, so the increase in High Density Advance Packaging (HDAP) usage will grow.

Extremely-high pin-count devices, such as ECUs, APUs, CPUs, GPUs, MCUs, and FPGAs, have changed the way engineers plan and implement each device's external interfaces, or I/Os. To meet overall component criteria, such as size, thickness, performance, power, and cost, design trade-offs must be made between the chip(s) and its package. Different form factors for similar end products also mandate that different board-level platforms be considered.

To resolve these challenges, many design teams are exploring cross-domain collaboration where the focus is on the optimized integration between and across the different implementation substrates involved (Figure 1). Through collaboration, design teams can achieve overall designs that efficiently meet size, performance, cost, yield, and power requirements.

Traditionally, many design teams have used spreadsheets, with the resultant, and often infamous, bump-ball map. Spreadsheets and bump-ball maps, however, are not design tools; they are simply documents that show the current state of design intent. As standalone documents, they are incapable of evaluating different scenarios, accurately modeling devices, or performing rule-based design optimization. Design intent is often misinterpreted or lost, and redundancy is often introduced into the flow and across design teams.

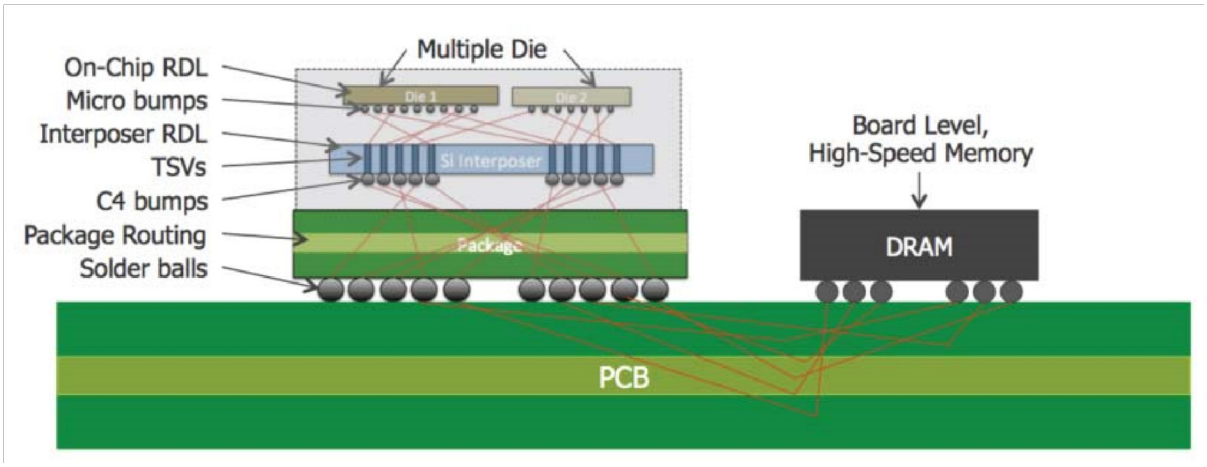

Figure 1: Designing complex HDAP should be an integrated process that allows for optimization across substrates.

This paper defines the key capabilities needed to build a formal, cross-substrate integration flow that enables full collaboration between the IC(s), package, and PCB and that includes multiple, target, board-level platforms for when devices/components are intended for use on different PCB form factors (Figure 2).

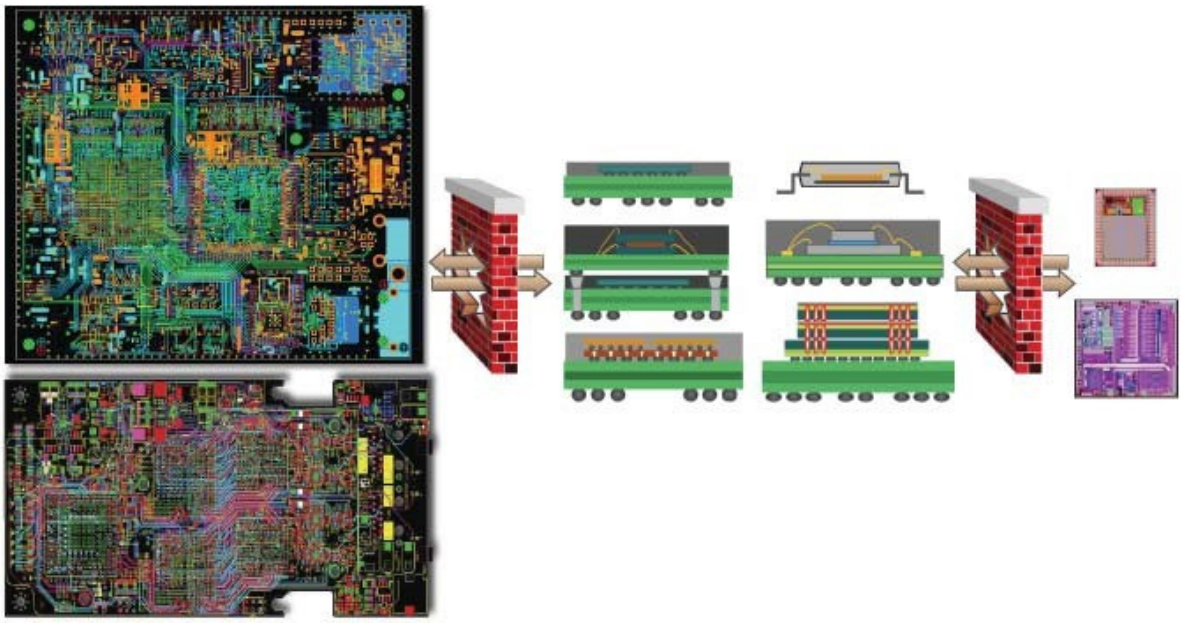

Figure 2: With a substrate integration prototyping approach, you can evaluate multiple packaging variables in the context of multiple PCB form factors. Alternatively, you could target a single device at multiple platforms and form factors. You can even perform board-driven ball-out planning.

PACKAGING VARIABLES

A common practice for minimizing cost and time-to-market is to use the same IC die in multiple end products. That sounds good but it does present problems. For example, a particular APU/CPU could be used in both a smart phone and a tablet but it's is a huge design challenge to determine the most cost-effective package that would perform equally in each platform. In another example, a GPU needs to work with memory devices provided by several vendors, each with its own pinout, but routing analysis is required to find the ideal BGA pin-out at the PCB level. There are plenty of other examples. How about providing multiple packaging options for the same IC based on specific customer needs? Could minor adjustments to a package's pin pitch lead to a more routable PCB, one with fewer routing layers?

Until recently, problems like these have been left to spreadsheets and white boards. Intelligent guesses were often the result. As with any informal "design flow," the results can be fraught with errors and risk redundancy…there is not much "prototyping exploration" with a spreadsheet! In addition, spreadsheet-based solutions restrict designs to a grid. Better is a gridless or "balls-anywhere" approach that allows for considerably more options and superior optimization (Figure 3).

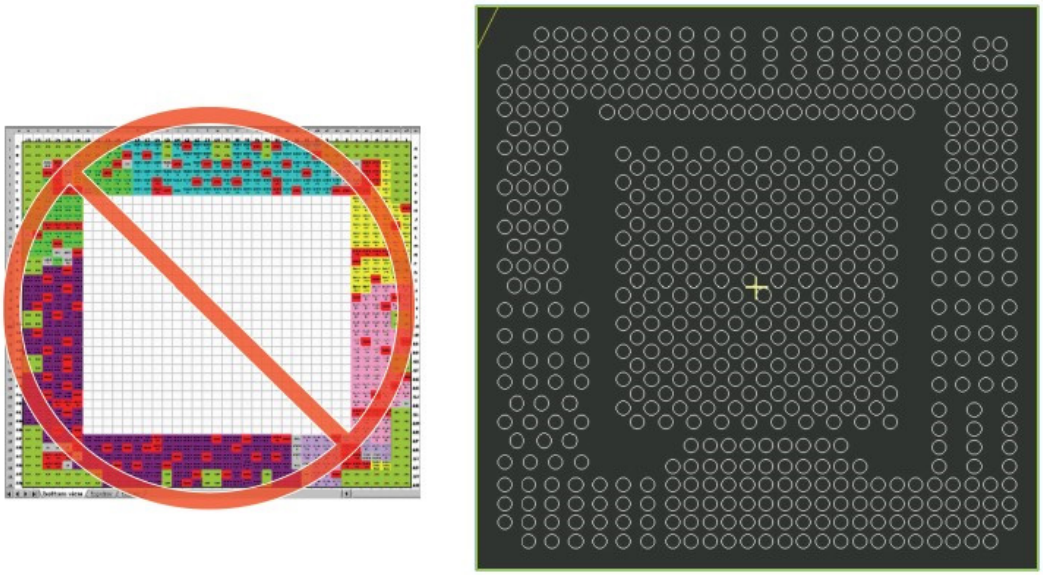

Figure 3: Spreadsheets limit ball layout to a pre-defined grid. A gridless or "balls-anywhere" tool allows balls to be moved and arranged for an optimal result.

WHAT SYSTEM INTEGRATION COULD LOOK LIKE

As stated earlier, many designers and design teams still use spreadsheets to manage the connectivity definition and assignment between the IC and the package. Given the accelerating rate of IC and package complexity and demands, these methods simply cannot keep up (Figure 4).

Even without increased complexity, there are many reasons why a better connectivity methodology is needed. An ideal system would enable the following:

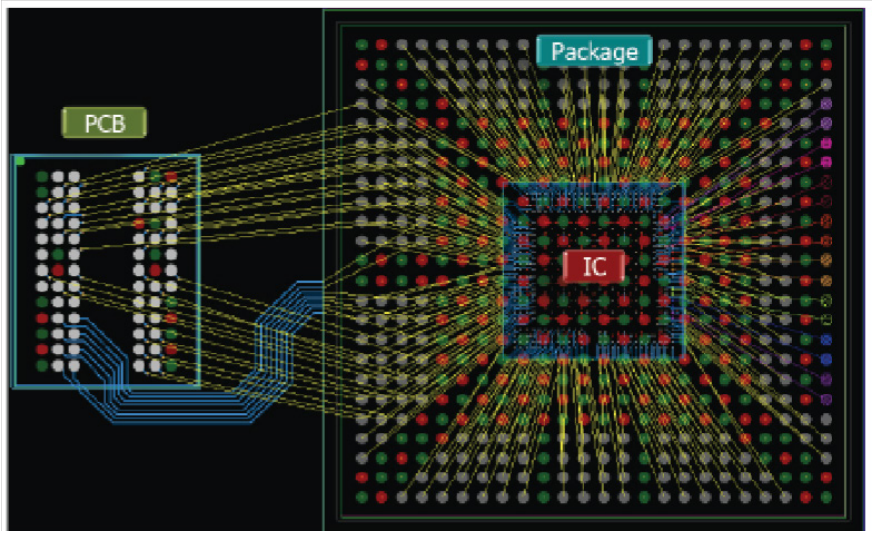

Figure 4: A good design flow should allow exploration of escape/breakout routing based pin assignments from the viewpoint of any of the substrate domains.

- WYSIWYG representation of an irregular-pitch BGA
- Display of connectivity and breakout/escape routing
- Assignment of connectivity optimization
- Rules-based pin assignment
- Direct integration with physical design and analysis tools
- The ability to manage ECO changes from ICs, interposers, package substrate, and PCB
- Dynamic pin adjustments
- Dynamic support for cross-substrate co-design optimization

MULTI-SUBSTRATE INTEGRATION

Multi-substrate interconnect prototyping, planning, and optimization is difficult. It requires the ability to model the floor plan and the I/O assignments of the IC, along with the package-substrate constraints and variables and multiple PCB platforms (form factors). Industry standards should be leveraged by individual domain: e.g., LEF/DEF for the IC data, and csv-formatted ASCII or AIF for the package-substrate data.

A good design flow also needs to provide engineers with the ability to visualize the complete system. Once the system has been captured, the flow must also compensate for cross-domain signal-naming conflicts and power/ground shorting (Figure 5).

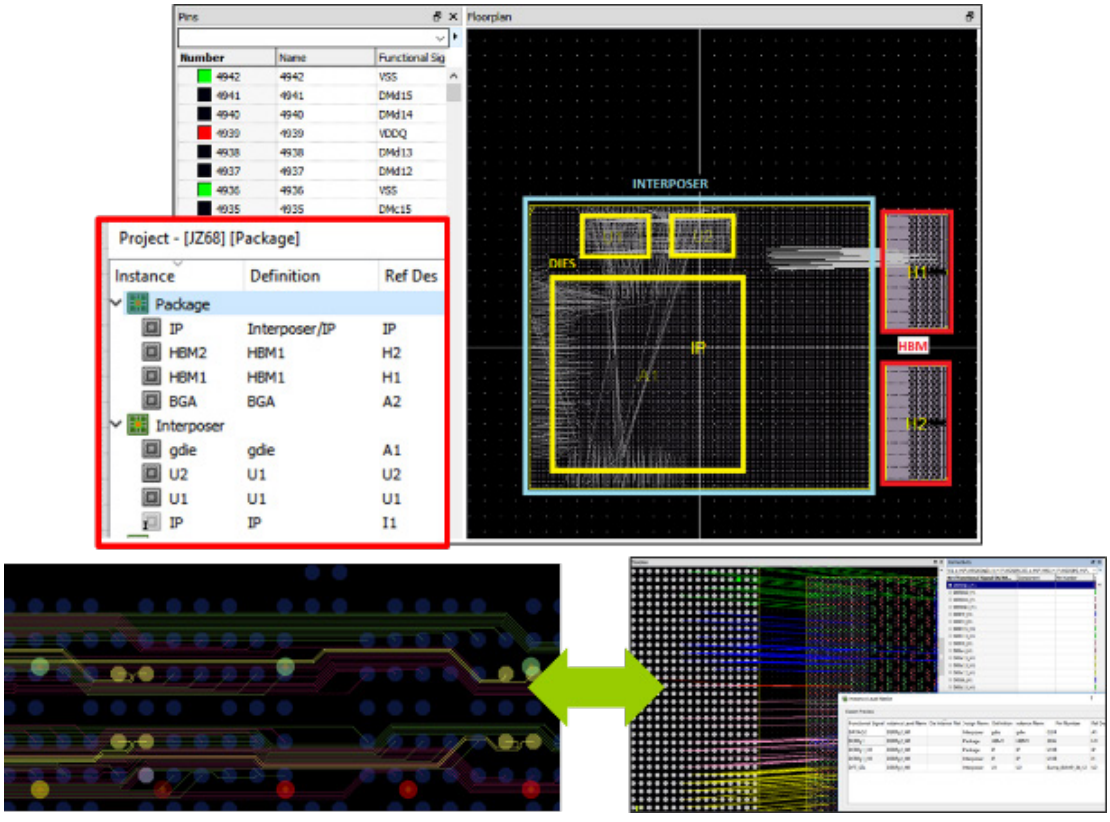

Figure 5: Constructing a system-level view from multiple data sources and design tools provides an environment for rapid prototype planning and route evaluation.

The flow should allow designers in each domain to use the design environment with which they are most comfortable, such as Verilog® for the chip designers and graphical schematics for the board designers.

The package pinout (ball and signal locations/assignments) typically has the most flexibility with respect to optimizing interconnect paths from the IC to the board. Unfortunately, not every pin on a package can be handled equally; for example, differential pairs must be kept together, signal-to- power ratios must be considered, and so forth. Therefore, rules should be deployed to control/guide the pin optimization. Pin-out optimization should also consider any escape and breakout routing performed by the package substrate designer or the board layout designer (Figure 6).

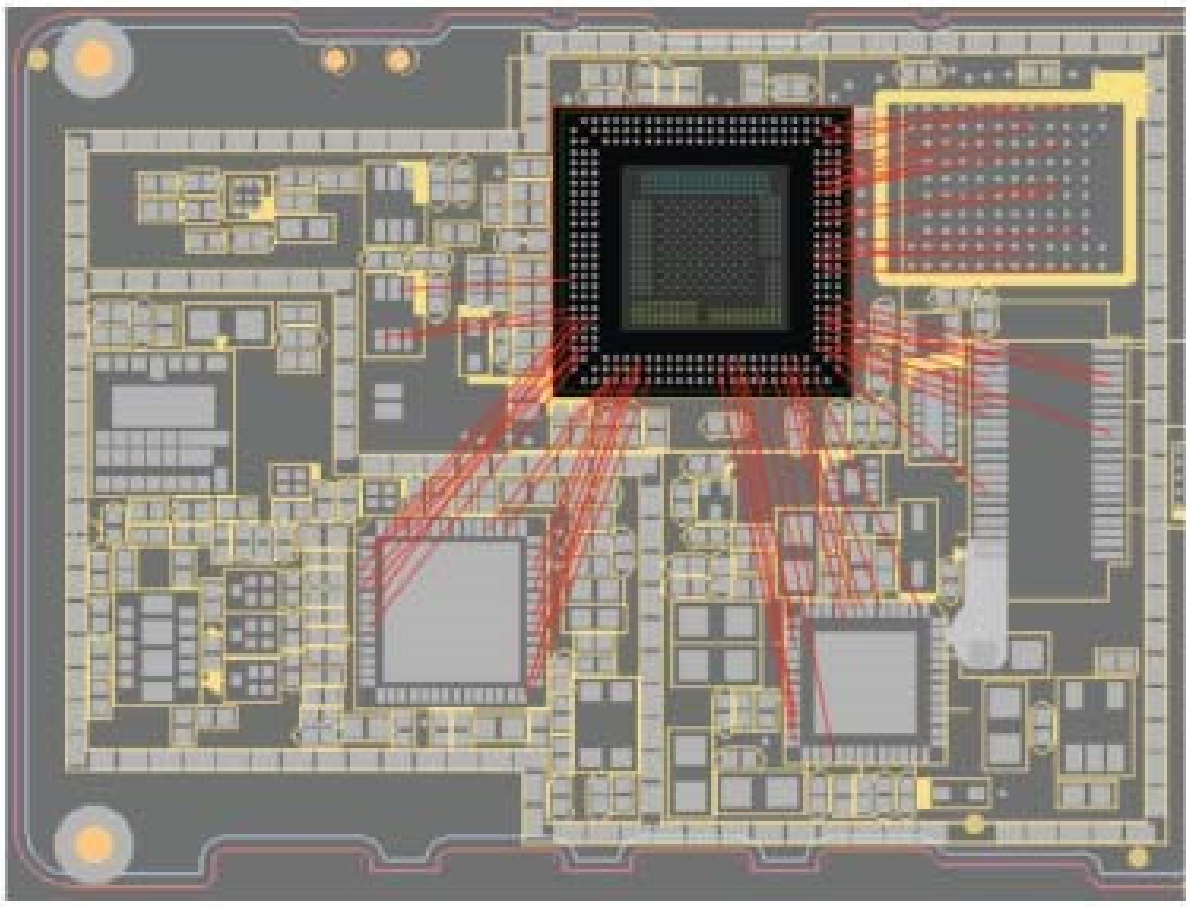

Figure 6: Finding the best package and pinout requires evaluation of multiple scenarios.

Evaluating multiple PCB scenarios simultaneously is critical when trying to determine the best package and pinout for multiple target applications. This is best achieved by adopting an integrated system that integrates multiple designs and scenarios as a single project.

SUMMARY

Many factors and challenges come into play when considering a true, multi-substrate integration flows for emerging HDAP design requirements. This paper highlighted many of them, including:

- Assembly and visualization of the complete system
- Multi-mode connectivity management
- Rules-based pin optimization
- Optimization with escape and breakout routing
- Support for multiple designs and platforms

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